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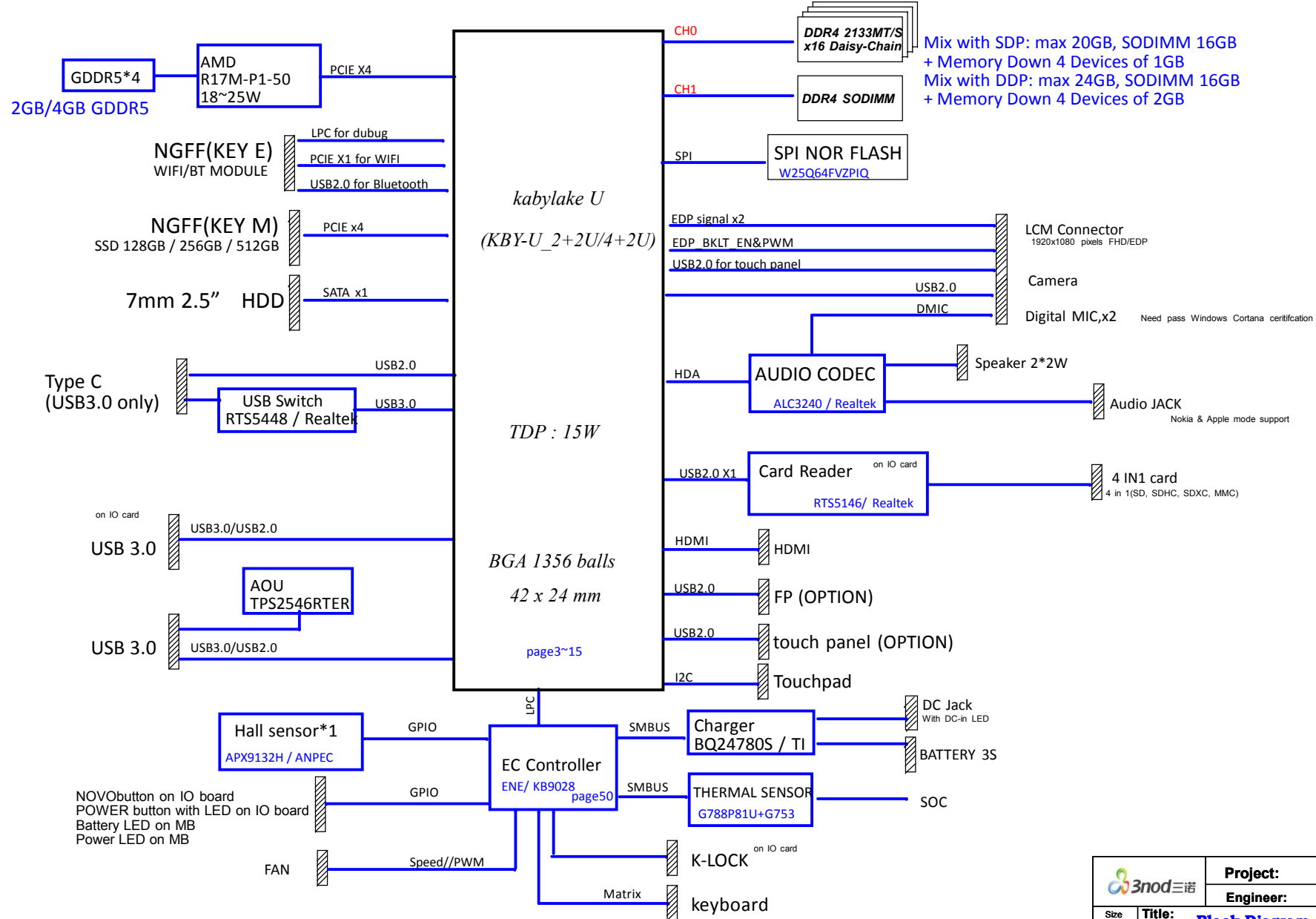
INTERNAL ONLY

BPAGE DRAWING

shy\_x\_rnd\_...  
Wed Jun 03 11:22:42 2015

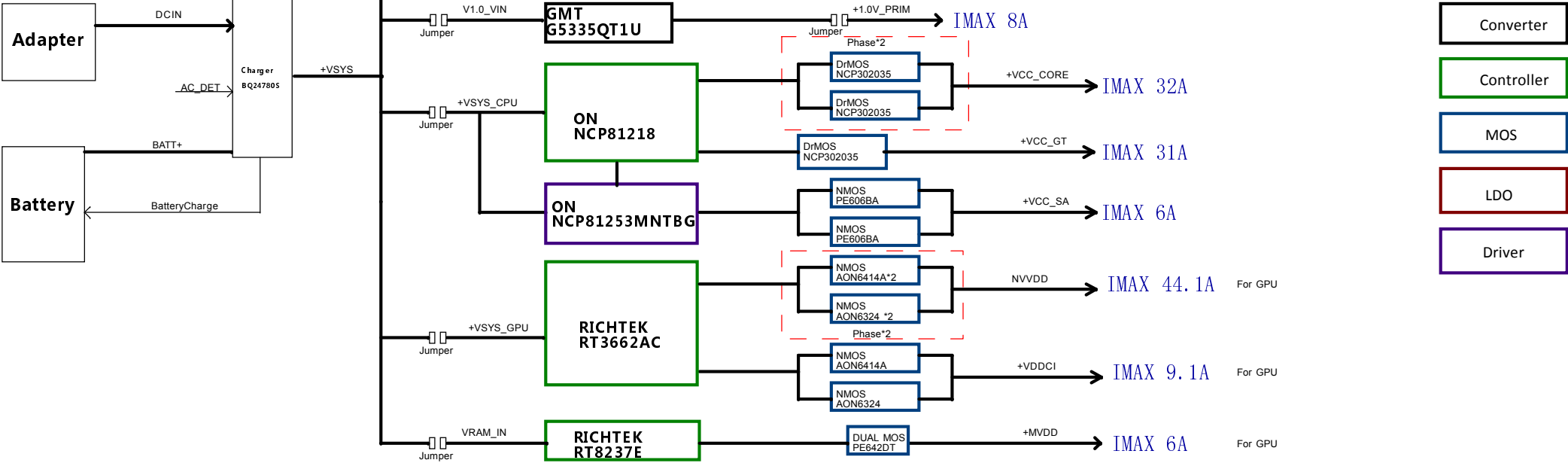
		Project: 330S-14&15	
		Engineer: Luffy	
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330S-14&15 for Lenovo



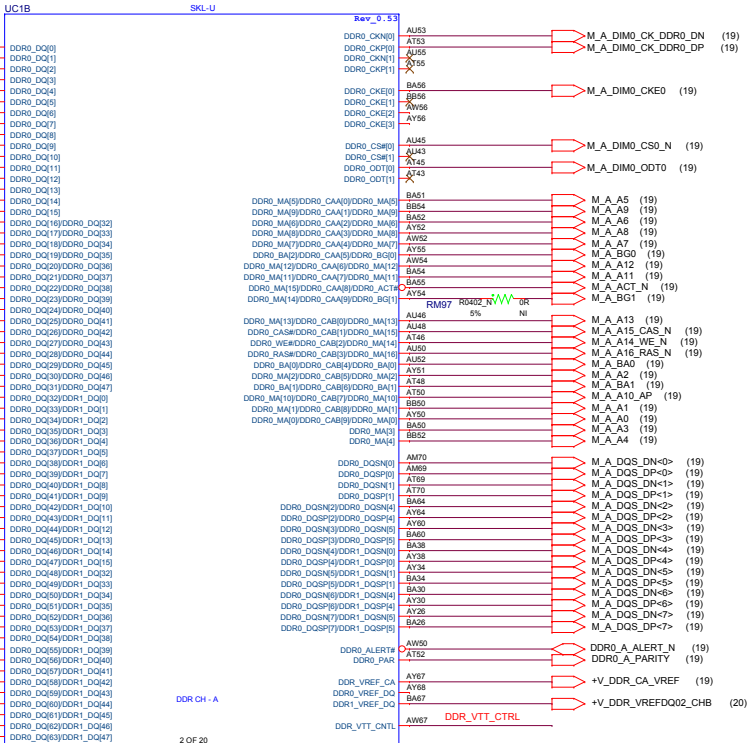
		Project:	330S-14&15
		Engineer:	Luffy
Size	Title: Block Diagram	Rev	
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# Power Map



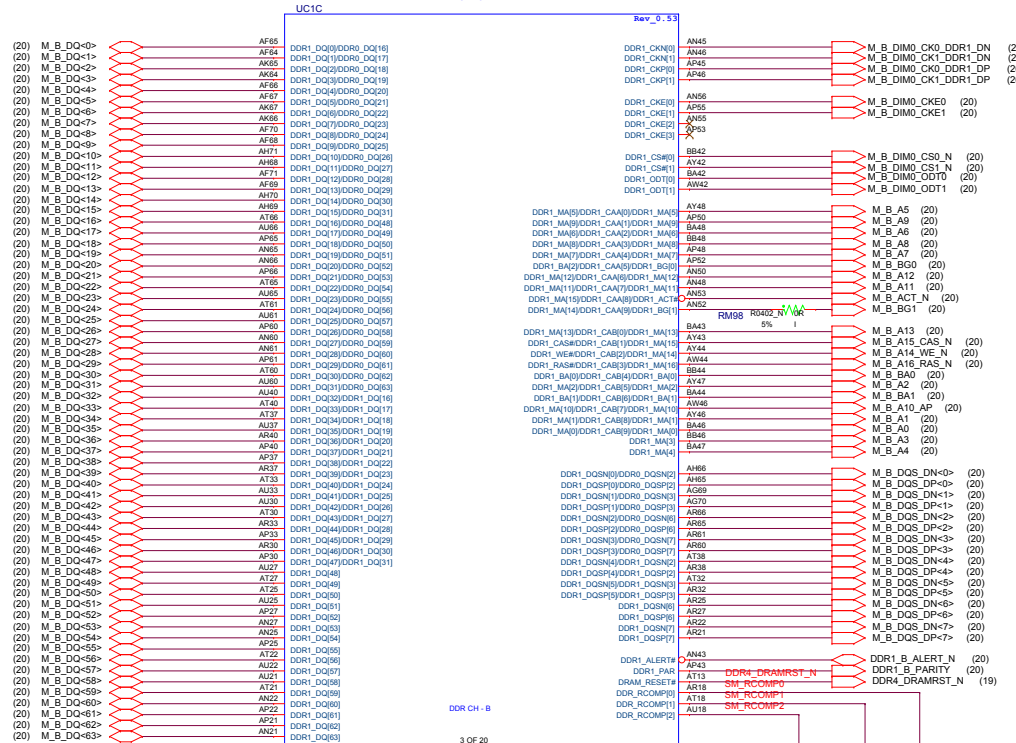


# Interleaved



SKL-U\_BGA1356  
<BOM Structure>

# Interleaved

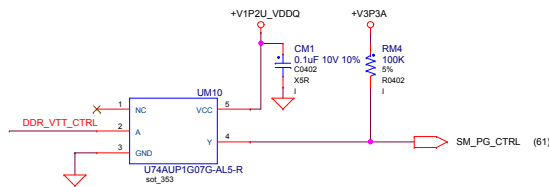


SKL-U\_BGA1356  
<BOM Structure>

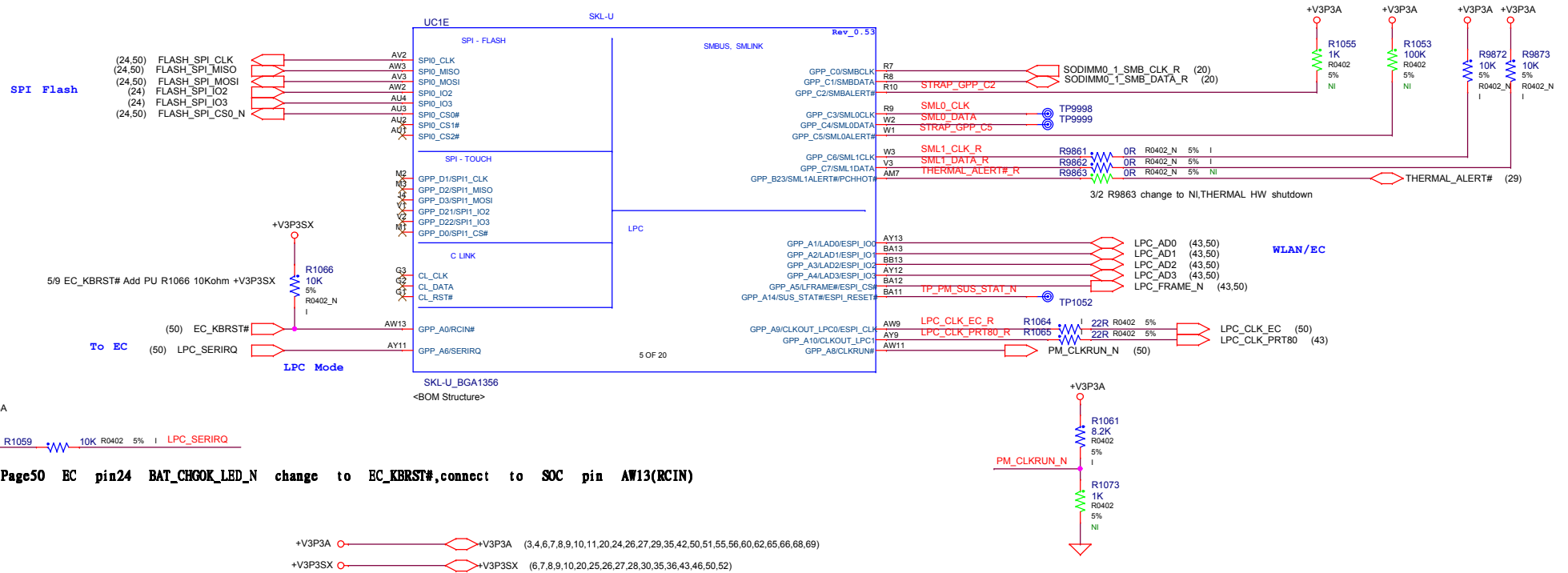
1. To support DDP, need to change two pins on DRAM. You have reserved them. Pls install the BOM.

	X16 SDP	X16 DDP TwinDie
DRAM M9 pin	VSS	Connect to CPU BG1
DRAM E9 Pin	VSS	U2Q

Memory size	4Gb or 8Gb	16Gb
DRAM M9 pin	RM95, RM96, RM97, RM98 need install	RM95, RM96, RM97, RM98 need install
DRAM E9 pin	RM99, RM100 need install	RM99, RM100 need install
SOC RCOMP0	RM79, RM81, RM83, RM85, RM87, RM89, RM91, RM93 need install 0 ohm	RM79, RM81, RM83, RM85, RM87, RM89, RM91, RM93 need install 240 ohm
	RM3 121 ohm need install	



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Size: Custom		Engineer: Luffy
Title: KBL-U(2/12)DDR4		Rev: v01
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5/9 Page50 EC pin24 BAT\_CHGOK\_LED\_N change to EC\_KBRST#,connect to SOC pin AW13(RCIN)

SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

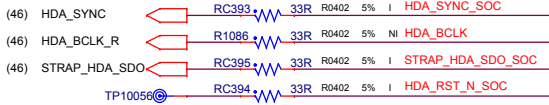
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = <b>LPC</b> Is selected for EC. (Default) 1 = <b>eSPI</b> Is selected for EC. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

### To Enable ME Override

(50) ME\_Flash\_EN  R9848 R0402\_N 5% I STRAP\_HDA\_SDO\_SOC

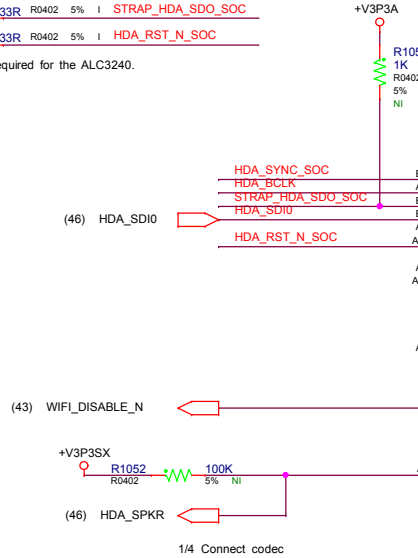
Difference with armour  
Add EC to enable ME override

5/23 R9848 install, BIOS request



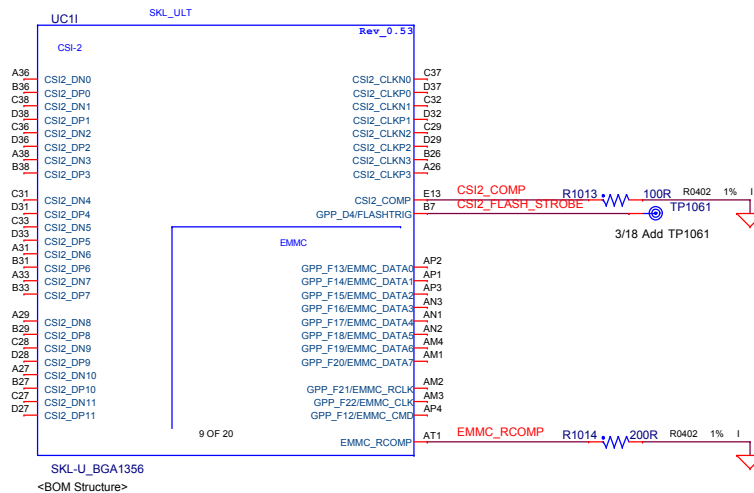
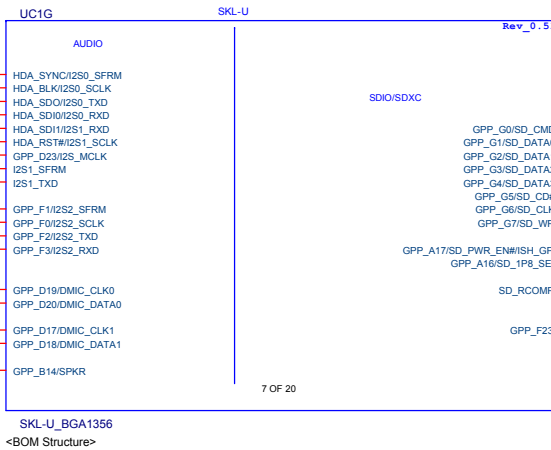
Note: RESET# is not required for the ALC3240.

### HDA for AUDIO



+V3P3A (3,4,5,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)

+V3P3SX (5,7,8,9,10,20,25,26,27,28,30,35,36,43,46,50,52)




5/10 Del TP1055,TP1056,TP1057,TP1058,TP1059,TP1060,TP1016,TP1017,  
MIPI differential don't test point

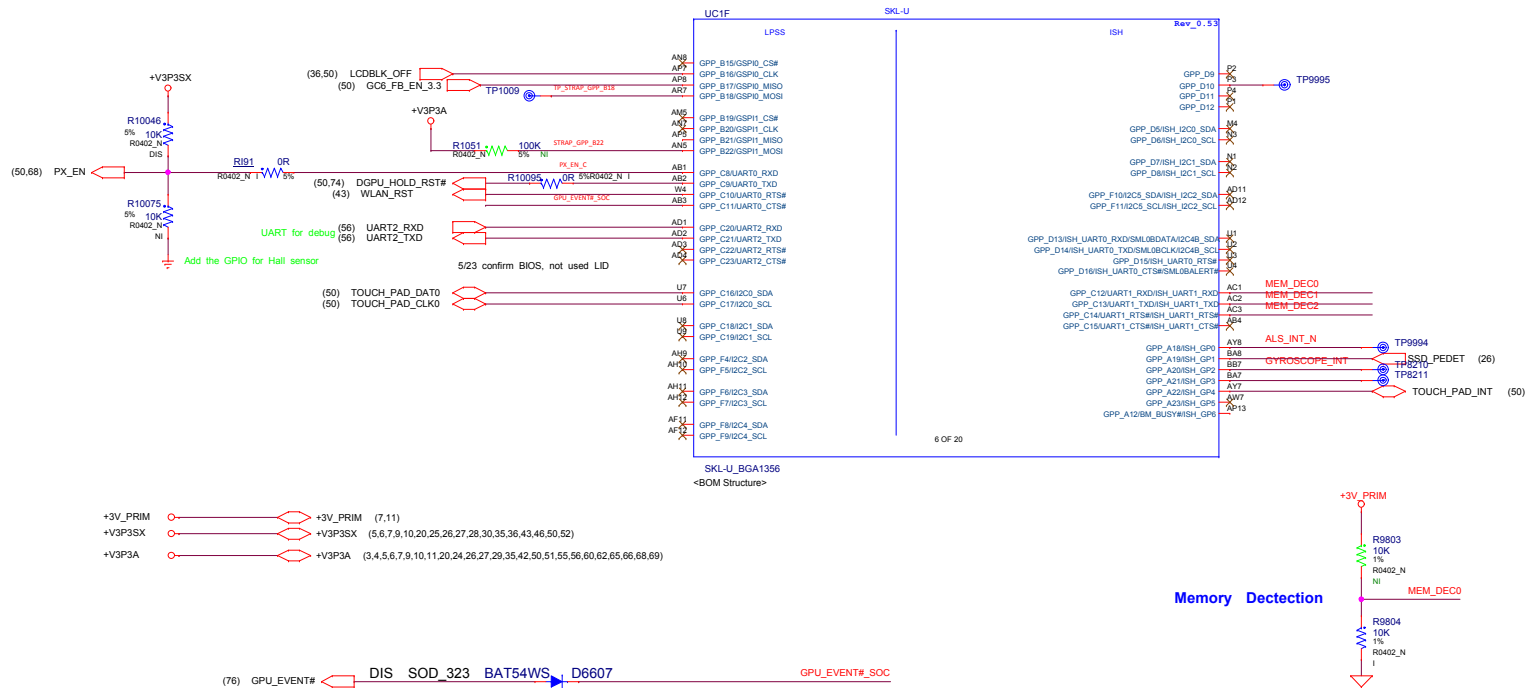
HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Enable</b> security measures defined in the Flash Descriptor. (Default)</p> <p>1 = <b>Disable</b> Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.</li><li>This signal is in the primary well.</li></ol>
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "Top Swap" mode. (Default)</p> <p>1 = <b>Enable</b> "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWIT or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>Software will not be able to clear the Top Swap bit until the system is rebooted.</li><li>The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4).</li><li>This signal is in the primary well.</li></ol>

Difference with armour  
Add 0ohm NI

TP1061

		<b>Project:</b>	330S-14&15
		<b>Engineer:</b>	Luffy
<b>Size</b>	<b>Title:</b>	KBL-U(4/12)HDA,EMMC,SD	
Custom		Rev	V01
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### Memory Detection

	Samsung_4GB	Micron_4GB	Hynix_4GB	Samsung_8GB	Micron_8GB	Hynix_8GB	Samsung_16GB	Micron_16GB
MEM_DEC0	0	1	0	1	0	1	0	1
MEM_DEC1	0	0	1	1	0	0	1	1
MEM_DEC2	0	0	0	0	1	1	1	1

Default

GSP10_MOS1 / GPP_B18	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "No Reboot" mode. (Default)</p> <p>1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>This signal is in the primary well.</li></ol>						
GSP11_MOS1 / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	<p>This Signal has a weak internal pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).</p> <table><thead><tr><th>Bit 6</th><th>Boot BIOS Destination</th></tr></thead><tbody><tr><td>0</td><td>SPI (Default)</td></tr><tr><td>1</td><td>LPC</td></tr></tbody></table> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.</li><li>Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.</li><li>This signal is in the primary well.</li></ol>	Bit 6	Boot BIOS Destination	0	SPI (Default)	1	LPC
Bit 6	Boot BIOS Destination								
0	SPI (Default)								
1	LPC								

Keyparts	Character	Supplier	Description	3NOD PN	Lenovo P/N
Lenovo B/S part sourcing plan					
CPU	Intel® 6th Gen Core™	Intel	i3-6100U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i3-6100U 2.3G/2C/3M intel)	457100266700	SSA0K07374
		Intel	i5-6200U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i5-6200U 2.3G/2C/3M intel)	457100266800	SSA0K07375
		Intel	i7-6500U 2.5G/2C/4M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i7-6500U 2.5G/2C/4M intel)	457100266900	SSA0K07377
DRAM	4Gbx16 DDR4 2400 SDRAM (单颗容量 0.5GB)	Samsung	K4A4G165WE-BCRC (MEMORY DDR4 2400 256Mx16 96FBGA K4A4G165WE-BCRC Samsung SM30L08878)	403670650600	SM30L08878
		Micron(Elpida)	MT40A256M16GE-083E-B		SM30L08871
		Hynix	H5AN4G6NAFR-UHC (MEMORY DDR4 2400 256M x 16 96ball FBGA H5AN4G6NAFR-UHC Hynix SM30L08876)	403670650800	SM30L08876
	8Gbx16 DDR4 2400 SDRAM (单颗容量 1GB)	Samsung	K4A8G165WB-BCRC (MEMORY DDR4 2400 512Mx16 96FBGA K4A8G165WB-BCRC Samsung SM30L08874)	403670650700	SM30L08874
		Micron(Elpida)	MT40A512M16JY-083E-B	403670650900	SM30L08877
		Hynix	H5AN8G6NAFR-UHC (MEMORY DDR4 2400 512M*16 96FBGA MT40A512M16JY-083E-B Micron SM30L08877)		SM30L08875

Project: 330S-14&15	
Engineer: Luffy	
Size: Custom	Title: KBL-U(6,12)GPIO
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GPU x4

SD Card

NGFF WiFi Module

HDD

NGFF SSD

Difference with armour  
SSD interface SATA change to PCIe  
SATA1A change to PCIe port 9,10,11,12

Checklist  
Gen1 and Gen2=100nF  
Gen3=220nF

## High Speed I/O (HSIO) Lane Multiplexing in SKL-U

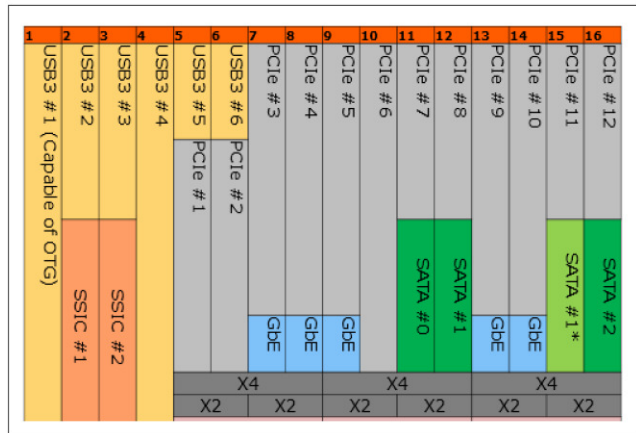


Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

+V3P3A +V3P3SX

(3,4,5,6,7,8,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)

(5,6,7,8,10,20,25,26,27,28,30,35,36,43,46,50,52)

SKL-U\_BGA1356  
<BOM Structure>

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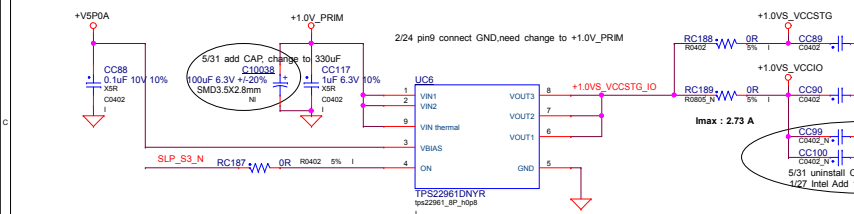
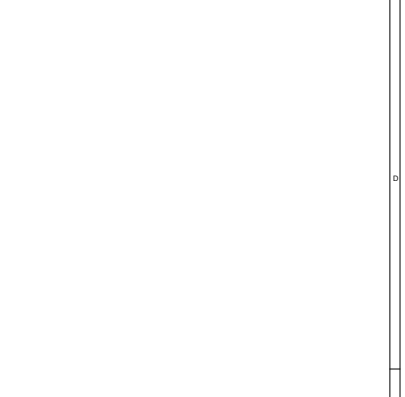
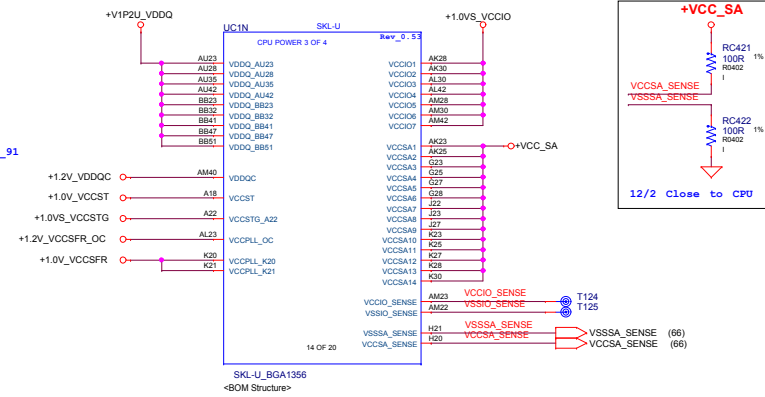
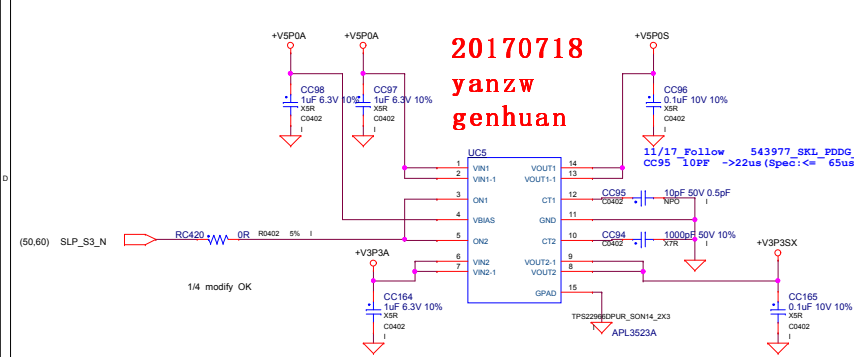
GPIO	DEVICE CONTROL
USB_OC0#	Type C
USB_OC1#	USB2 Port 2
USB_OC2#	NA
USB_OC3#	WWAN_PWR_ON
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NGFF SSD KEY M
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	SSD_SATA_PCIE_DET_N

NOTE:  
USE FITC TO ALLOW SELECTION OF  
PCIe VS SATA BASED ON STRAPPING:

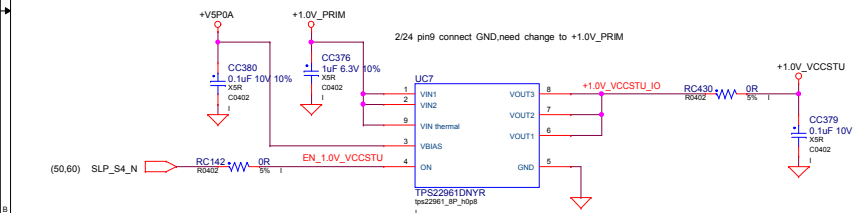
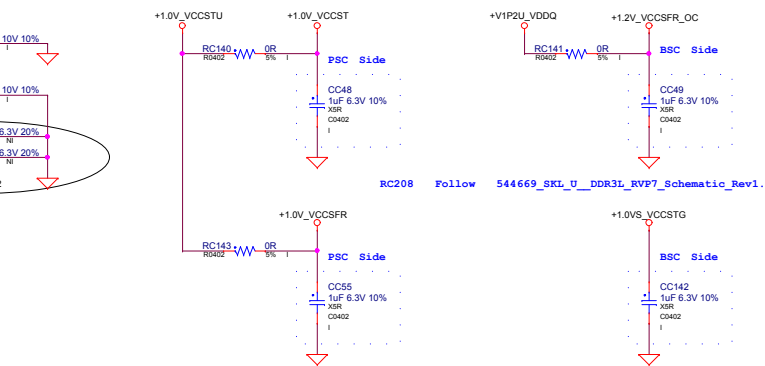
GPIO\_E\_2 FOR SATA2/PCIe:  
1 - SATA2, 0 - PCIe P9,P10,P11,P12

		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: KBL-U(7/12)PCIE,USB,SATA	Rev	
Custom		V01	
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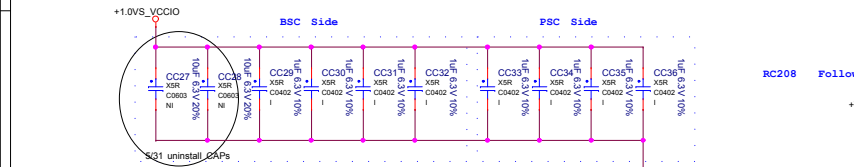
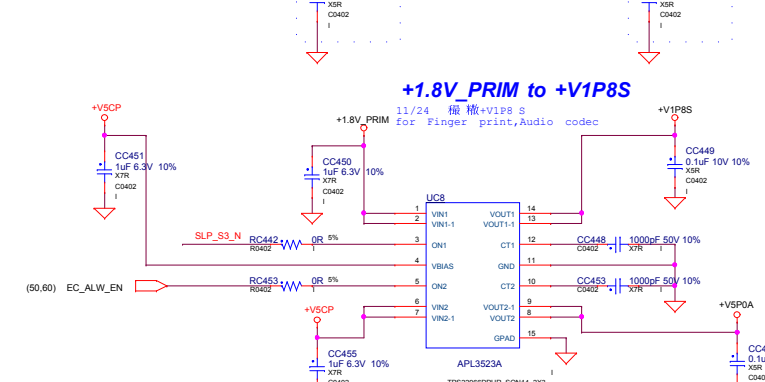
20170718  
yanzw  
genhuan



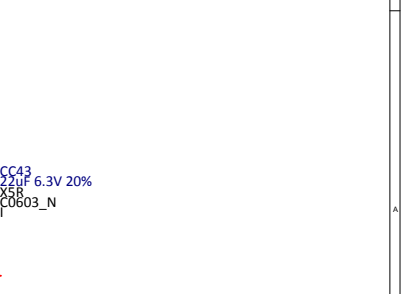
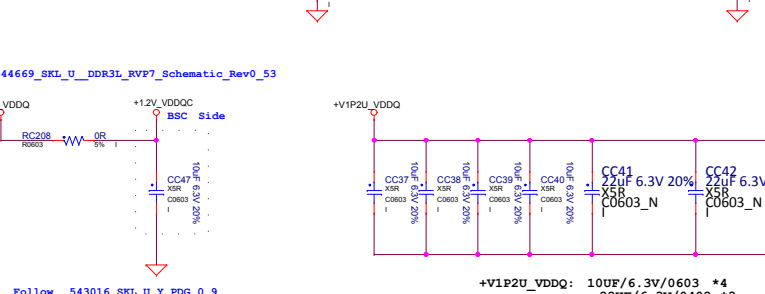
+1.0V\_PRIM to +1.0VS\_VCCSTG / +1.0VS\_VCCIO



+1.0V\_PRIM to +1.0V\_VCCSTU



RC208 Follow 544669\_SKL\_U\_DDR3L\_RVP7\_Schematic\_Rev0\_53



- +VCC\_SA (15.67)
- +V1P8S (68)
- +VSCP (42.60)
- +1.8V\_PRIM (11.48, 56.65)
- +V3P5A (5.4, 5.6, 7.8, 11.20, 24.26, 27.29, 35.42, 50.51, 55.56, 60.62, 65.66, 68.69)
- +V5P0S (25.30, 35.36, 46)
- +V5P0A (11.24, 27.50, 54.61, 62.63, 65.66, 67.68, 69.70, 72)
- +1.0V\_PRIM (11.14, 63)
- +V3P5X (5.6, 7.8, 10.25, 26.27, 28.30, 35.36, 43.46, 50.52)
- +V1P2U\_VDDQ (4.19, 20.21, 61.68)
- +1.0VS\_VCCSTG (3.12)
- +1.0VS\_VCCIO (3.14)

CC47 Follow 543016\_SKL\_U\_Y\_PDG\_0\_9

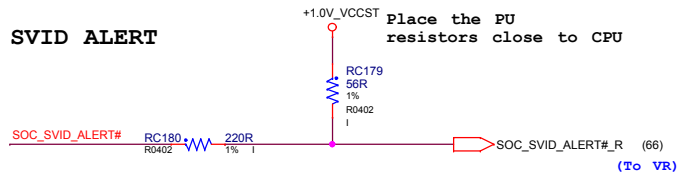
+V1P2U\_VDDQ: 10UF/6.3V/0603 \*4  
220UF/6.3V/0402 \*3

3nod 三诺		Project:	330S-14415
		Engineer:	Luffy
Size	Title: KBL-U(8/12)Power	Rev	V01
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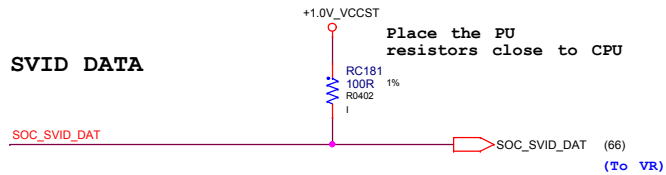


For CPU2+3e SKU

## SVID ALERT



## SVID DATA

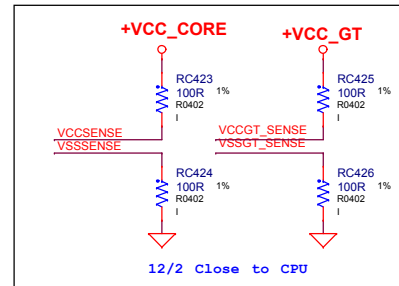


+VCC\_CORE (15,23,67)  
+1.0V\_VCCSTG (3,10)  
+VCC\_GT (15,67)  
+1.0V\_VCCST (3,7,10,14,66)

Trace Length < 25 mils

(66) VCCGT\_SENSE  
(66) VSSGT\_SENSE

Trace Length < 25 mils

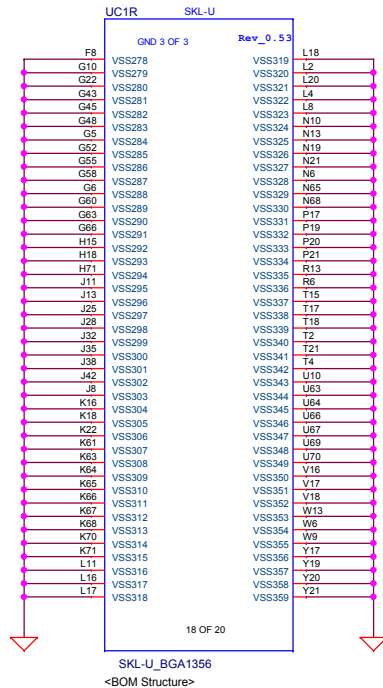
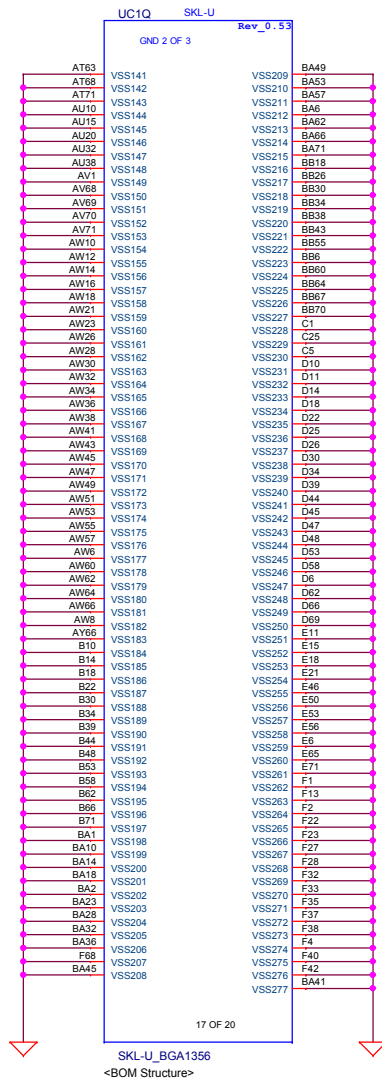
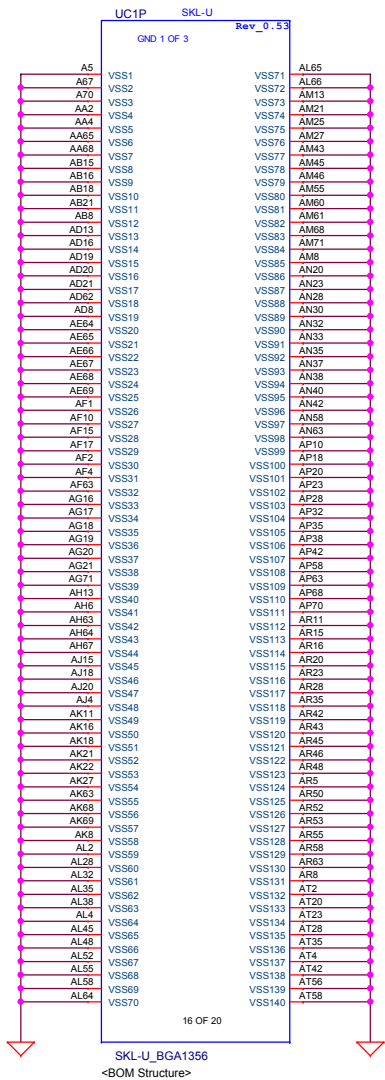


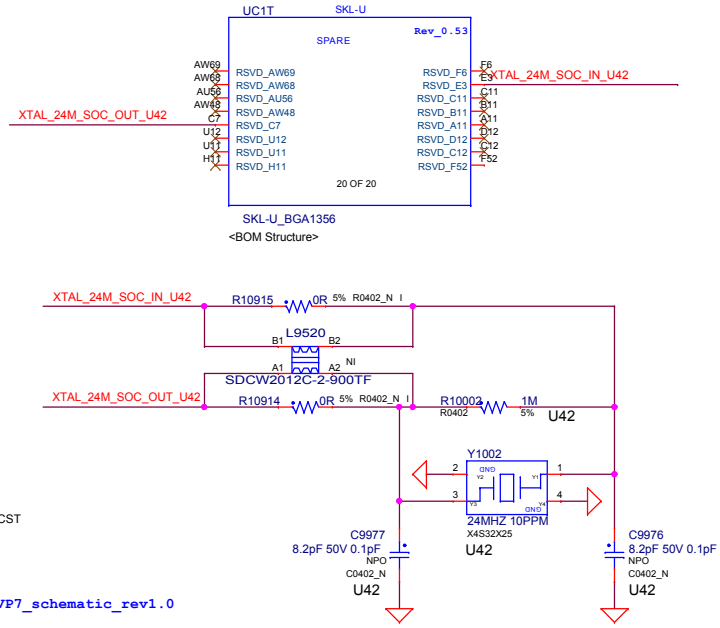
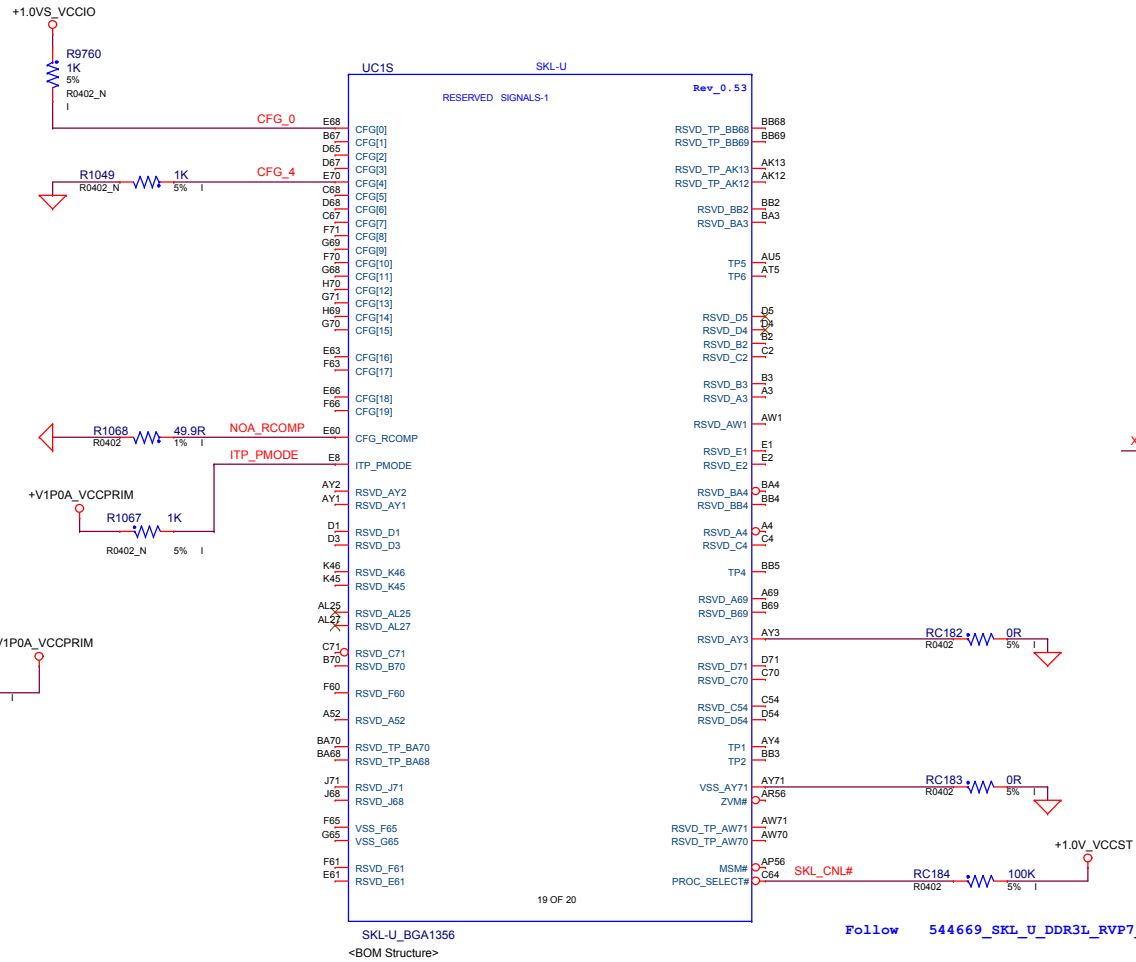
## Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
VccGT_SENSE / VssGT_SENSE			
VccGTx_SENSE / VssGTx_SENSE			
VccSA_SENSE / VssSA_SENSE			
VccIO_SENSE / VssIO_SENSE[1]		NA	

Note: [1] Does not apply when rails are merged.

		Project:	330S-14&15
		Engineer:	Luffy
Size	Title	Rev	
Custom	KBL-U(10/12)Power,SVID	V01	
Date:	Tuesday, September 26, 2017	Sheet	12 of 81






- +1.0VS\_VCCIO (3,10)
- +V1P0A\_VCCPRIM (7)
- +1.0V\_PRIM (10,11,63)
- +1.0V\_VCCST (3,7,10,12,66)

For 2+3e Solution  
PM\_ZVM#  
PM\_MSM#

Follow 544669\_SKL\_U\_DDR3L\_RVP7\_schematic\_rev1.0

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port  0 : Enabled; An external Display Port device is connected to the Embedded Display Port

		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: KBL-U(12/12)RSVD	Rev	
Custom		V01	
Date:	Tuesday, September 26, 2017	Sheet	14 of 81



CHANNEL-1:  
SA0:0  
SA1:1  
SA2:0

SA2\_CHB\_DM1  
SA1\_CHB\_DM1  
SA0\_CHB\_DM1

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

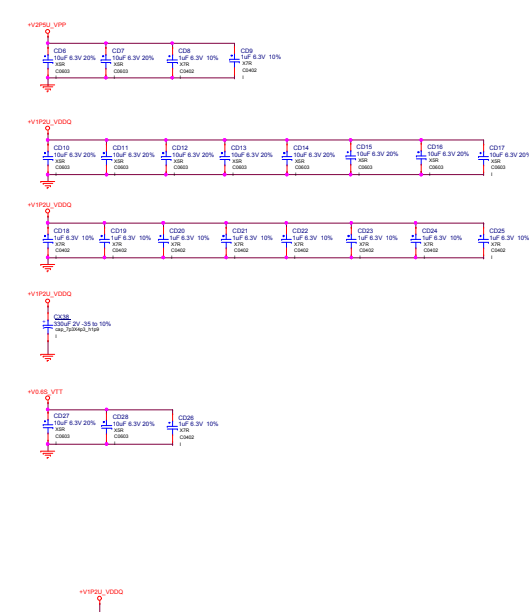
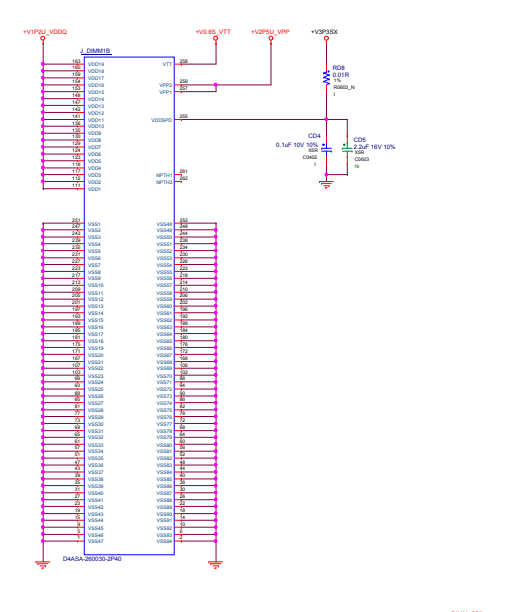
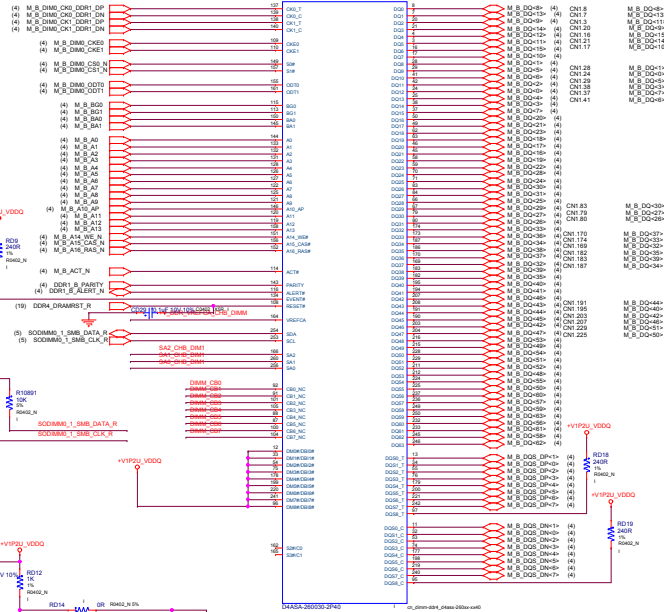
0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

0.1uF 10V 10%  
C02  
0.2uF 10V 10%  
C03  
0.1uF 10V 10%  
C04

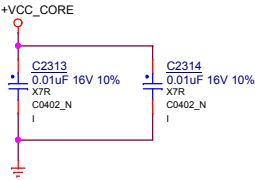


+VFP2L\_VDDQ  
+V8B5\_VTT  
+VFP5L\_VFP  
+VFP5B\_V




RF Solution

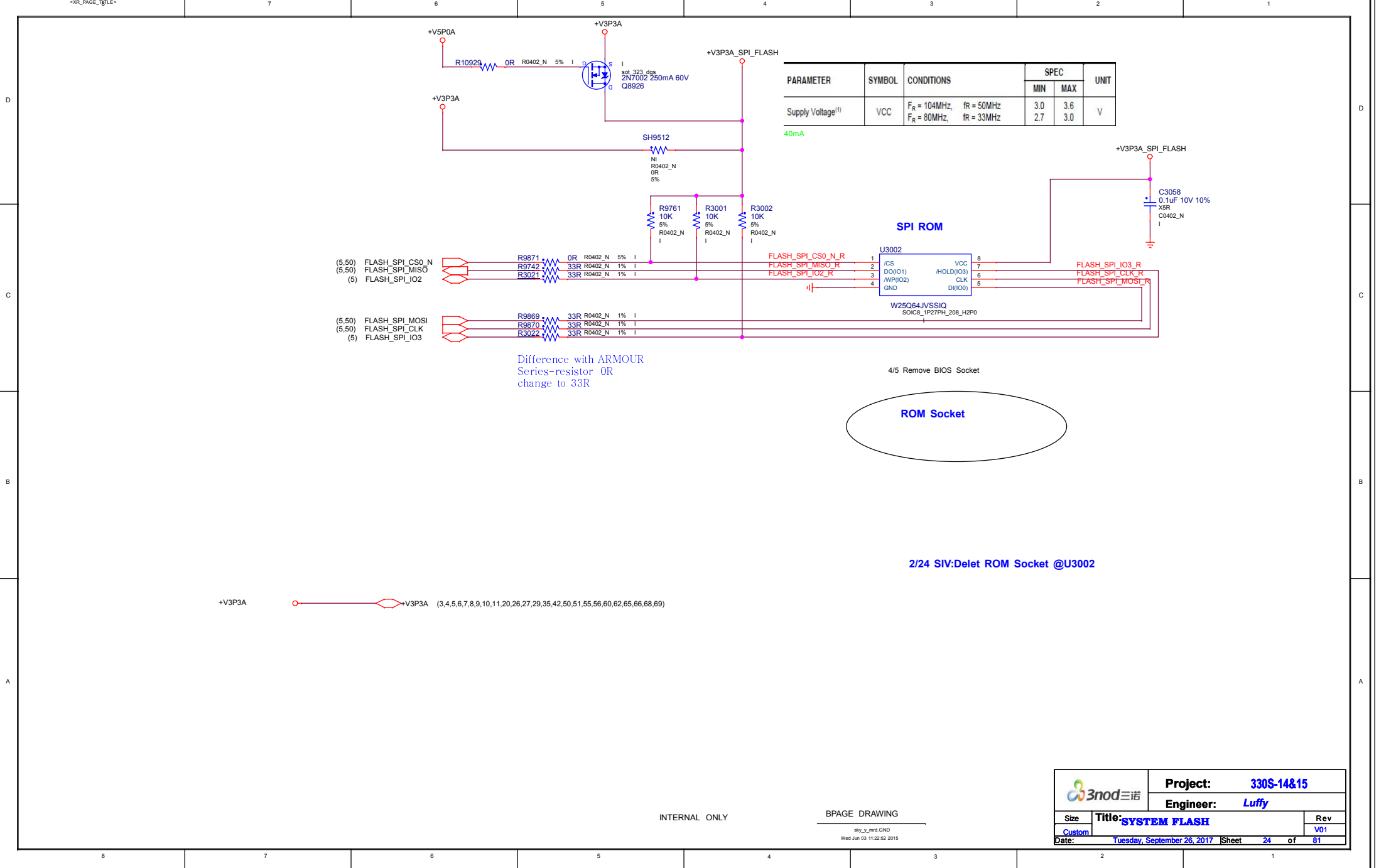
Cross Moat Cap.



EMC Solution



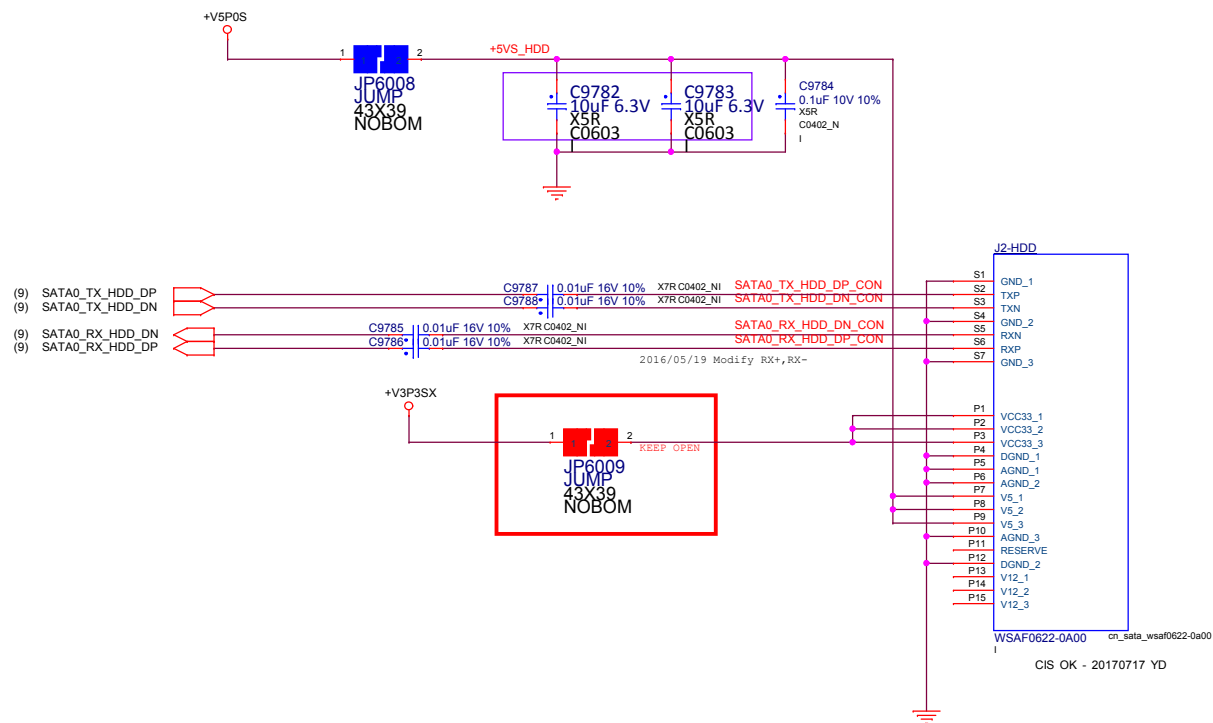
		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: RF / EMC Solution		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet 23 of	81



PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage <sup>(1)</sup>	VCC	F <sub>r</sub> = 104MHz, F <sub>r</sub> = 80MHz,	3.0 2.7	3.6 3.0	V

U3002	W25Q64JVSSIQ	SOIC8_1P27PH_208_H2P0
1	/CS	VCC
2	DO(I/O1)	/HOLD(I/O3)
3	/WP(I/O2)	CLK
4	GND	DI(I/O0)


		Project:	330S-14&15
		Engineer:	Luffy
Size	Title: SYSTEM FLASH		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	24 of 81



INTERNAL ONLY

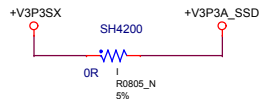
BPAGE DRAWING

sky\_y.med.GND  
Wed Jun 03 11:22:52 2015

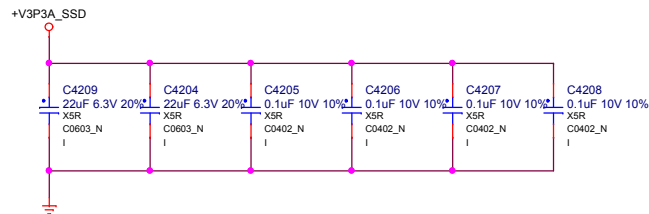
		Project: 330S-14&15	
Size		Engineer: Luffy	
Custom	Title: HDD	Rev	
Date: Tuesday, September 26, 2017		Sheet 25 of 81	
		V01	

# M.2 SSD Module

1. 4A @ADATA 128GB SSD  
2. 6A @ADATA 256GB SSD



Change SH4200 0805 shunt to resistor



PCIE12 RX  
follow intel CRB

Difference with armour  
SSD interface SATA change to PCIE  
If install SATA CARD,R4200,R4201 need install 0.01uF  
C0606,C0607 need install 0.01uF

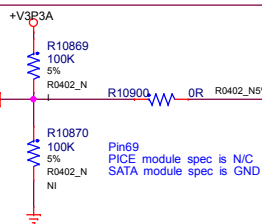
NGFF SSD module interface	PCIE	SATA
Reference	R4200,R4201 install 0ohm C0606,C0607 install 0.22uF	R4200,R4201 install 0.01uF C0606,C0607 install 0.01uF
Detect pin	R1050 install 10Kohm R1087 uninstall 100Kohm	R1050 uninstall 10Kohm R1087 install 100Kohm

Default

3/16 Add SSD(PCIE or SATA) BOM option table

Co-lay PCIE12 RX,reserved R4202,R4203  
please close to R4200,R4201

20170718  
yanzw  
genhuan



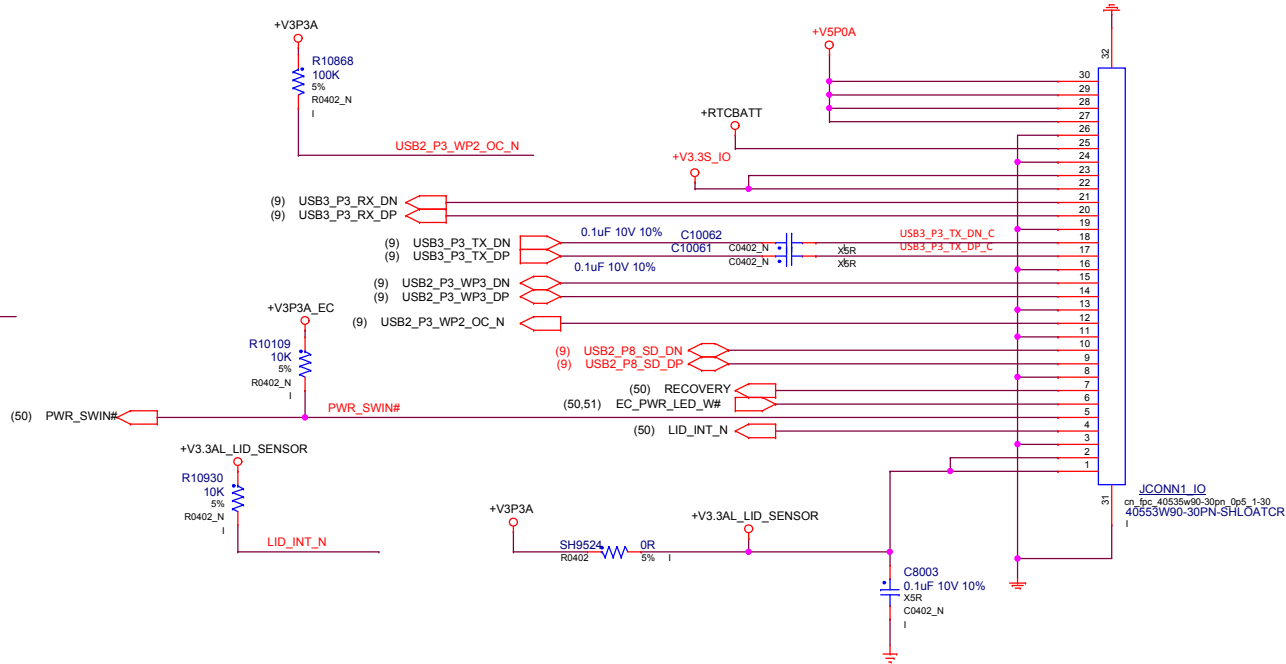
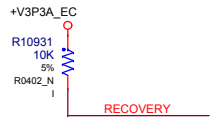
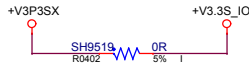
+V3P3SX (5,6,7,8,9,10,20,25,27,28,30,35,36,43,46,50,52)


INTERNAL ONLY

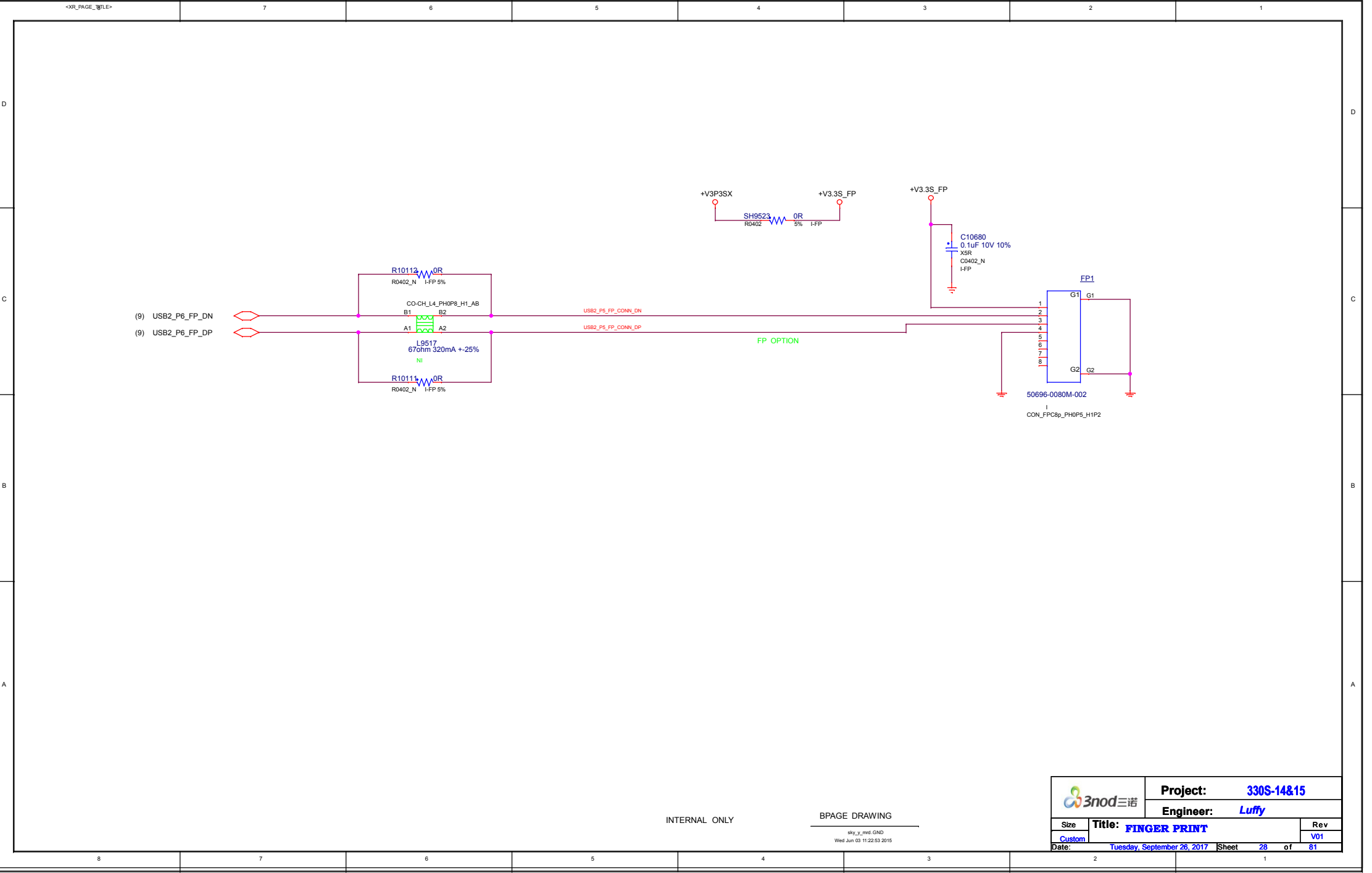
BPAGE DRAWING

shy\_x\_mtd +V3P3.26  
Wed Jun 03 11:22:52 2015

3nod 三诺		Project:	330S-14&15
		Engineer:	Luffy
Size	Title: PCIE SSD MODULE	Rev	V01
Custom			
Date:	Tuesday, September 26, 2017	Sheet	26 of 81




		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: IO CONNECTOR		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	27 of 81



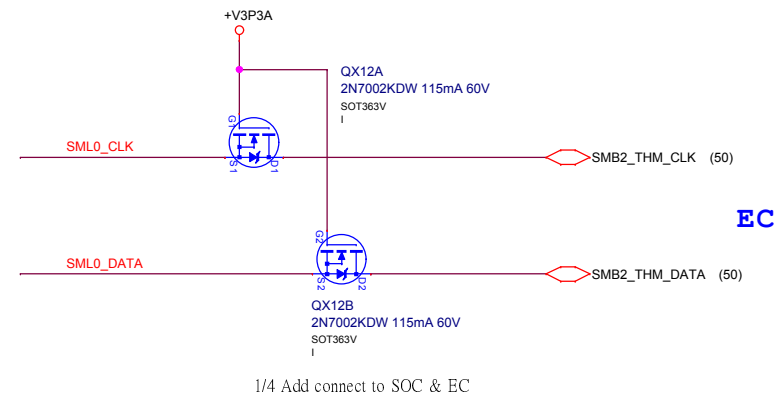
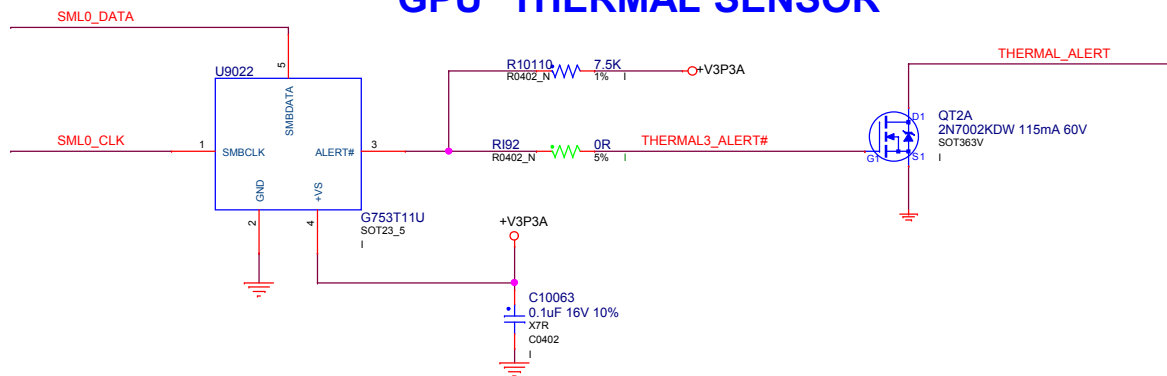
INTERNAL ONLY

BPAGE DRAWING

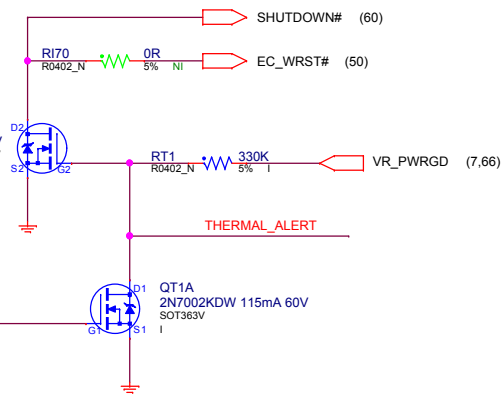
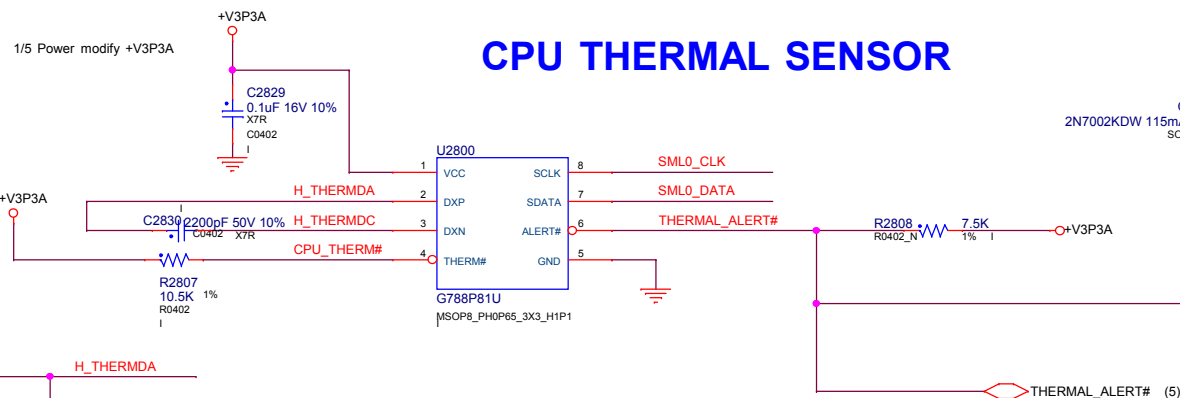
sky\_y\_mtd.GND  
Wed Jun 03 11:22:53 2015

		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: FINGER PRINT		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet 28 of	81

## GPU THERMAL SENSOR



## CPU THERMAL SENSOR



## CHARGE THERMAL SENSOR

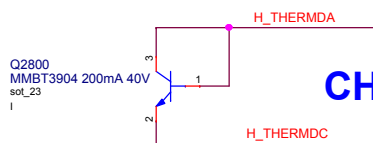
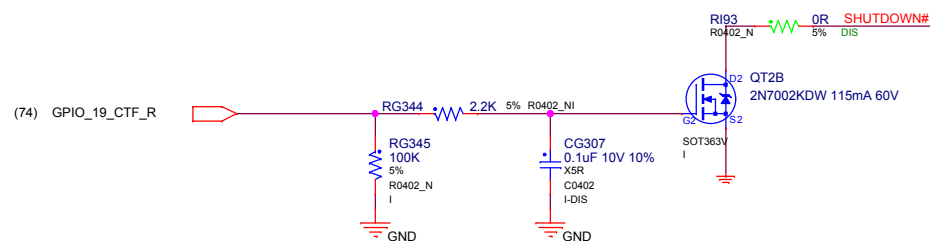


Table 10. Remote temperature THERM limit

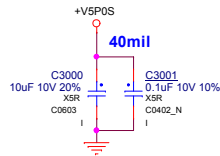
The default value is trapping after power up 100ms by different pull-up resistors of THERM and ALERT pin:

TEMPERATURE (°C)		THERM					
ALERT#	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ		
	77	87	97	107	117		
	79	89	99	109	119		
	81	91	101	111	121		
	83	93	103	113	123		
	85	95	105	115	125		

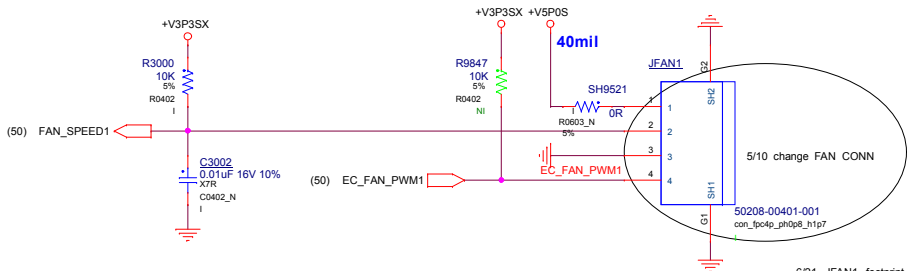


+V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,35,42,50,51,55,56,60,62,65,66,68,69)

		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: CPU THERMAL SENSOR	Rev	
B		V01	
Date:	Tuesday, September 26, 2017	Sheet	29 of 81



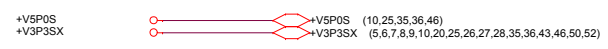
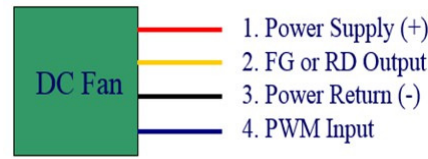
3/7 R9847 connect to +V5P0S,change to +V3P3SX



**FAN conn**  
6/21 JFAN1 footprint CON\_FPC4P\_PH0P6\_H1P55 change to con\_wtb\_4p\_ph0p6\_h1p55\_50376

CIS ok

1/11 Update FAN pin define



		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: FAN conn		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	30 of 81

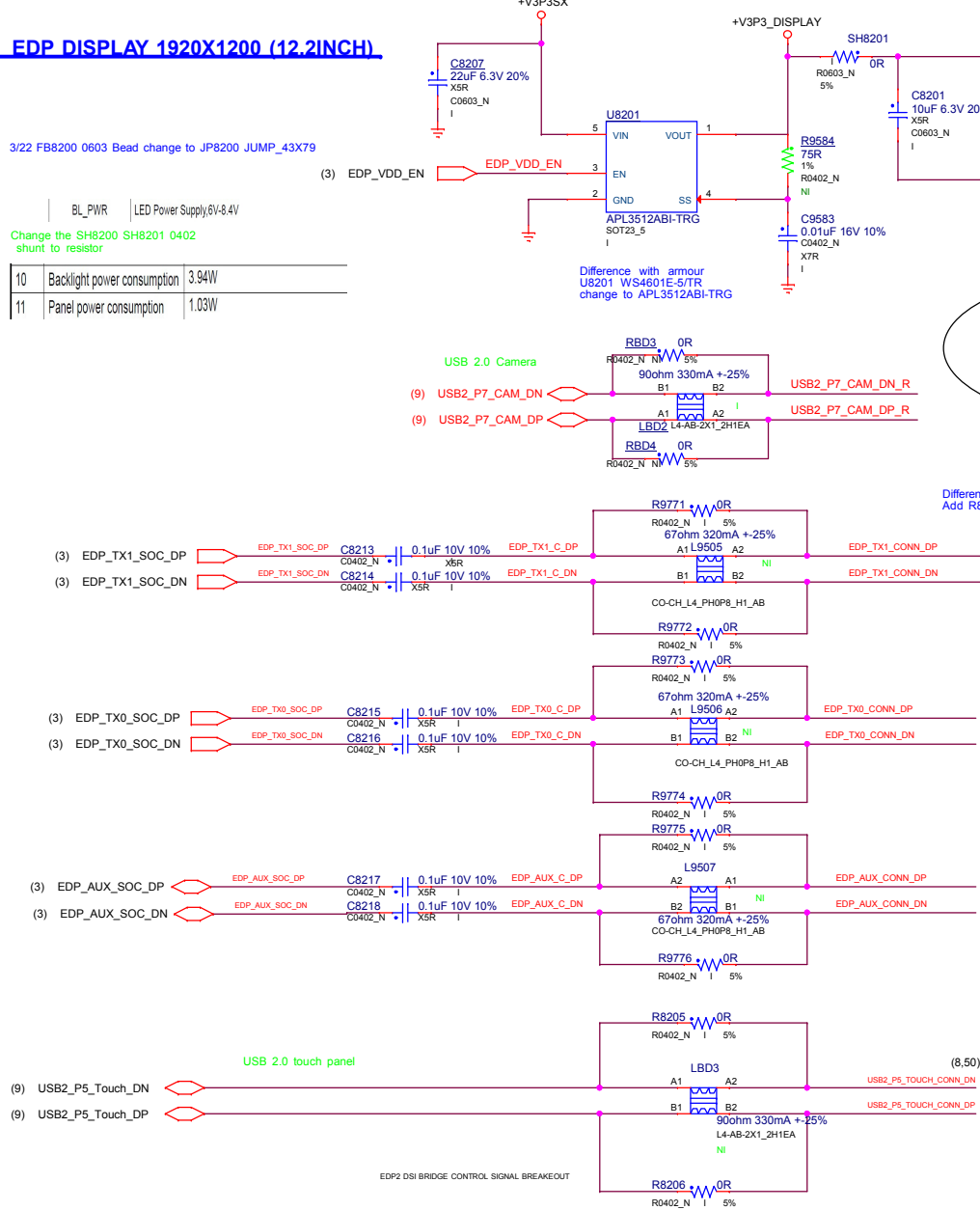


## EDP DISPLAY 1920X1200 (12.2INCH)

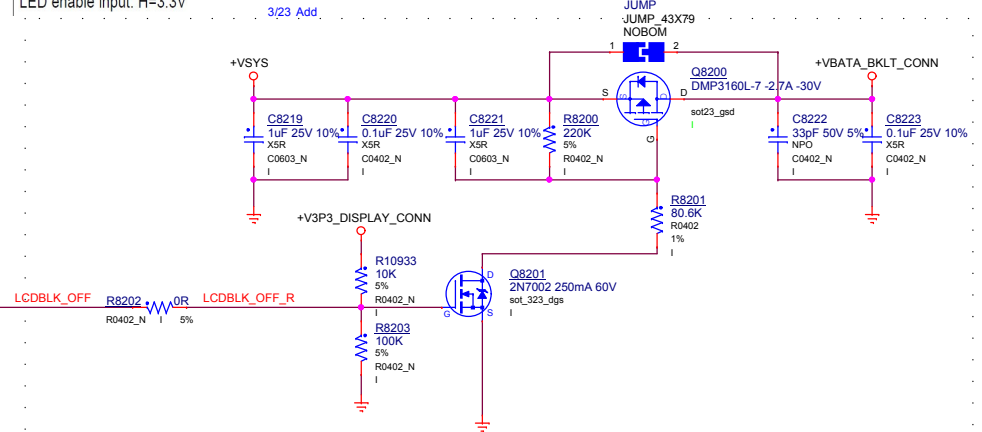
3/22 FB8200 0603 Bead change to JP8200 JUMP\_43X79

BL\_PWR LED Power Supply 6V-8.4V  
Change the SH8200 SH8201 0402  
shunt to resistor

10	Backlight power consumption	3.94W
11	Panel power consumption	1.03W



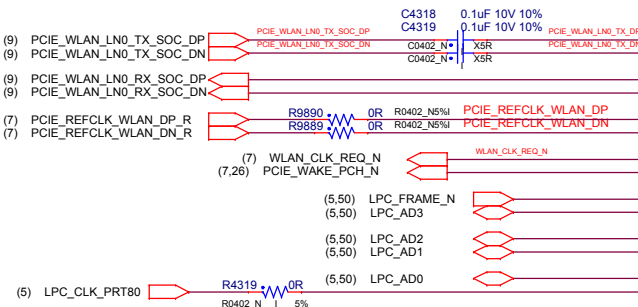
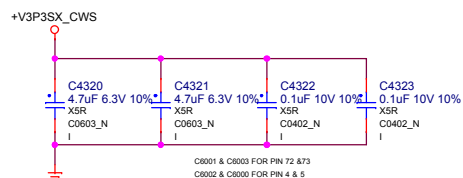
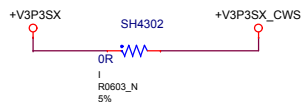
BL_PWM_DIM	LED PWM signal input. H=3.3V
BL_ENABLE	LED enable input. H=3.3V



3nod三诺		Project: 330S-14&15	
Custom		Engineer: Luffy	
Size	Title: DISPLAY	Rev	
Date: Tuesday, September 26, 2017	Sheet 36 of 81	V01	

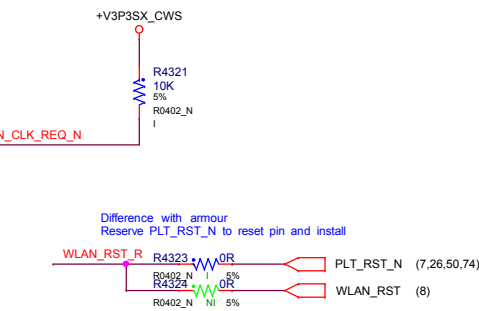
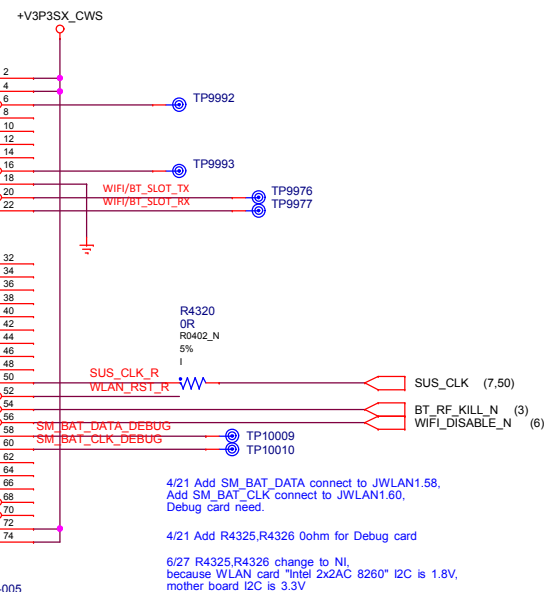


# WIFI & BT Module



2/16 change CONN

CIS ok

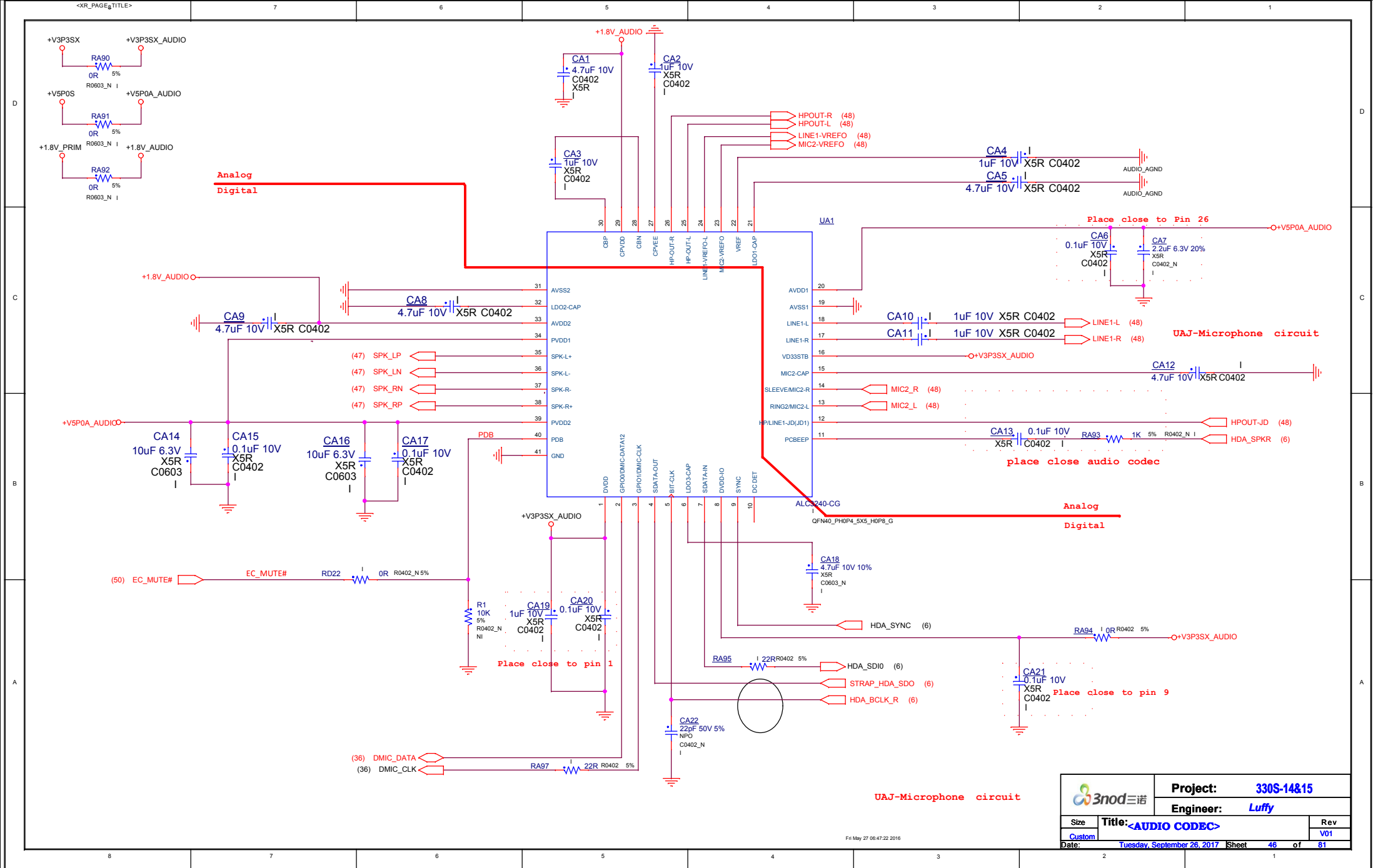


INTERNAL ONLY

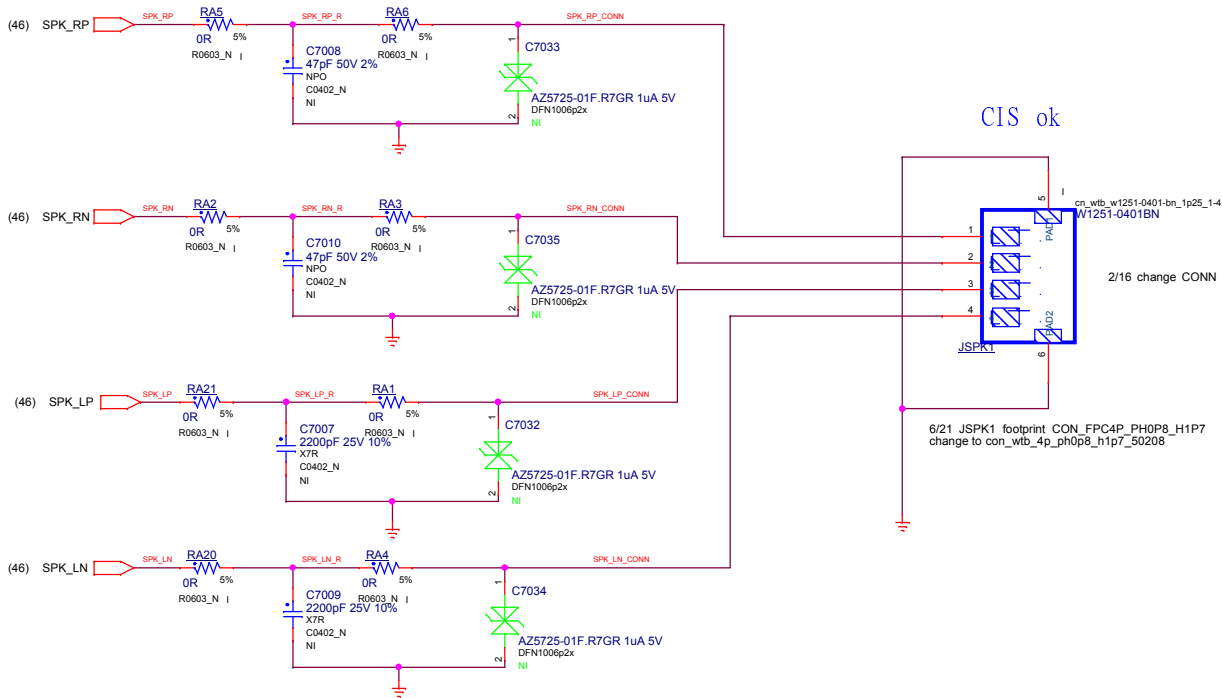
BPAGE DRAWING

shy\_y\_mms-V3P3\_43  
Wed Jun 03 11:23:00 2015

		Project: 330S-14&15
		Engineer: Luffy
Size: Custom	Title: WLAN WIFI BT MODULE	Rev: V01
Date: Tuesday, September 26, 2017	Sheet: 43	of 81




Speaker



INTERNAL ONLY

BPAGE DRAWING

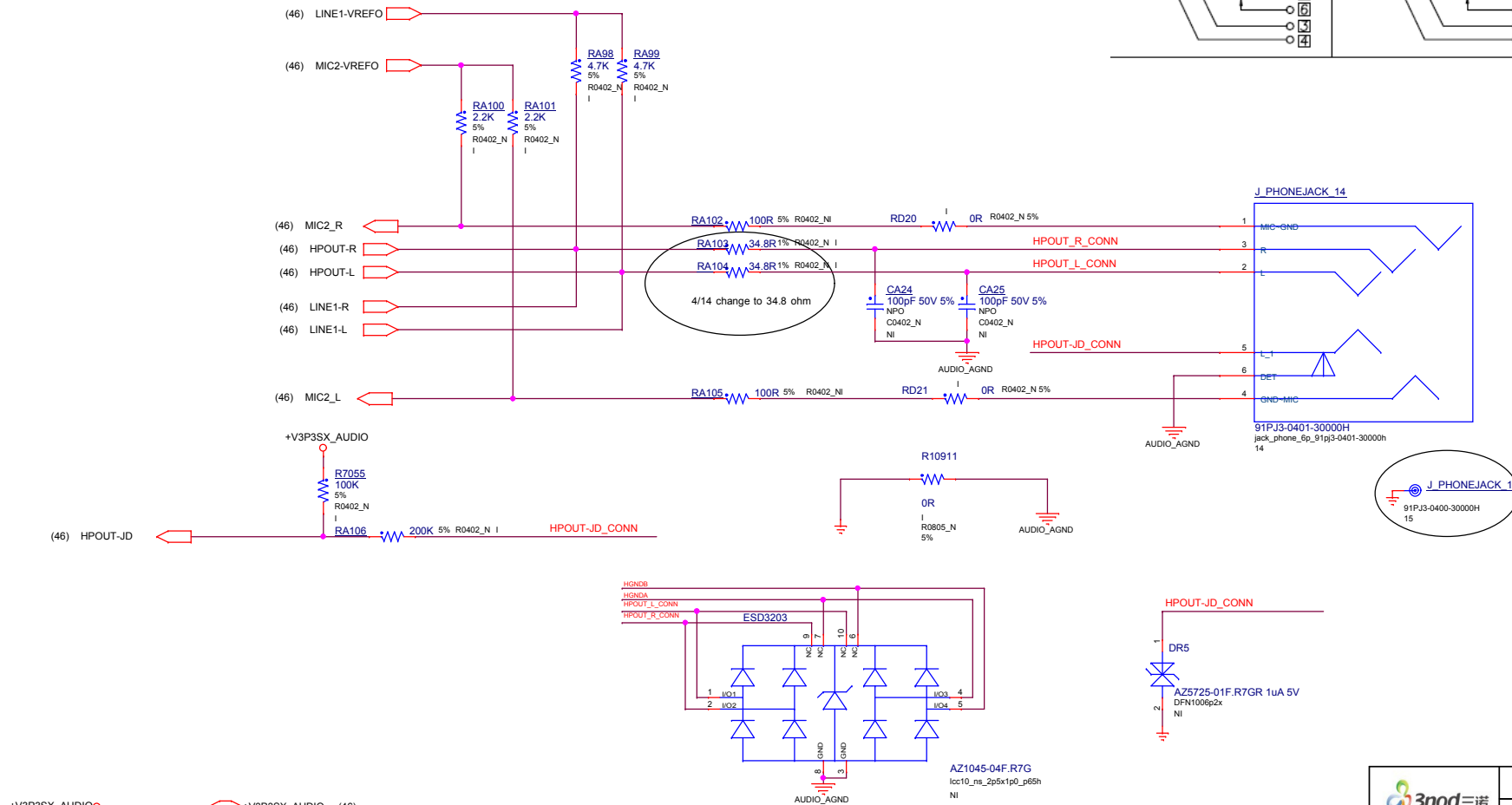
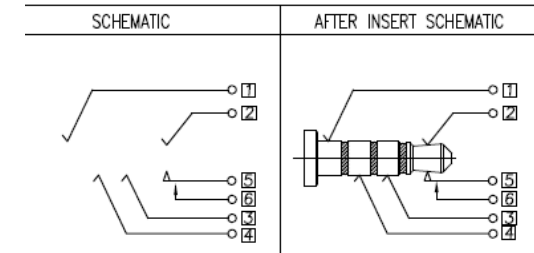
sky\_y\_msd.GND  
Wed Jun 03 11:23:02 2015

		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: Speaker	Rev	
Custom			
Date:	Tuesday, September 26, 2017	Sheet	47 of 81

## HEADSET JACK (Supports CTIA and OMTP headsets)

### Important:

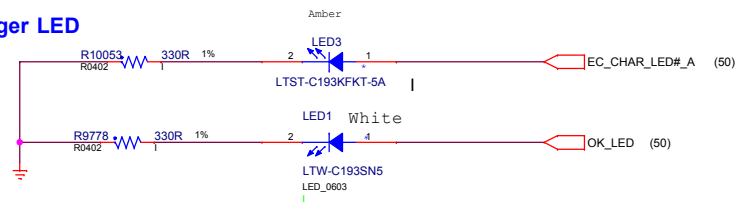
To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.



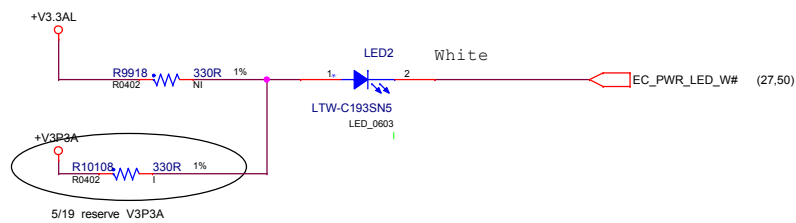
		Project: 330S-14&15
		Engineer: Luffy
Size: Custom	Title: <AUDIO_HEADSET>	Rev: V01
Date: Tuesday, September 26, 2017	Sheet: 48	of 81




### Charger LED

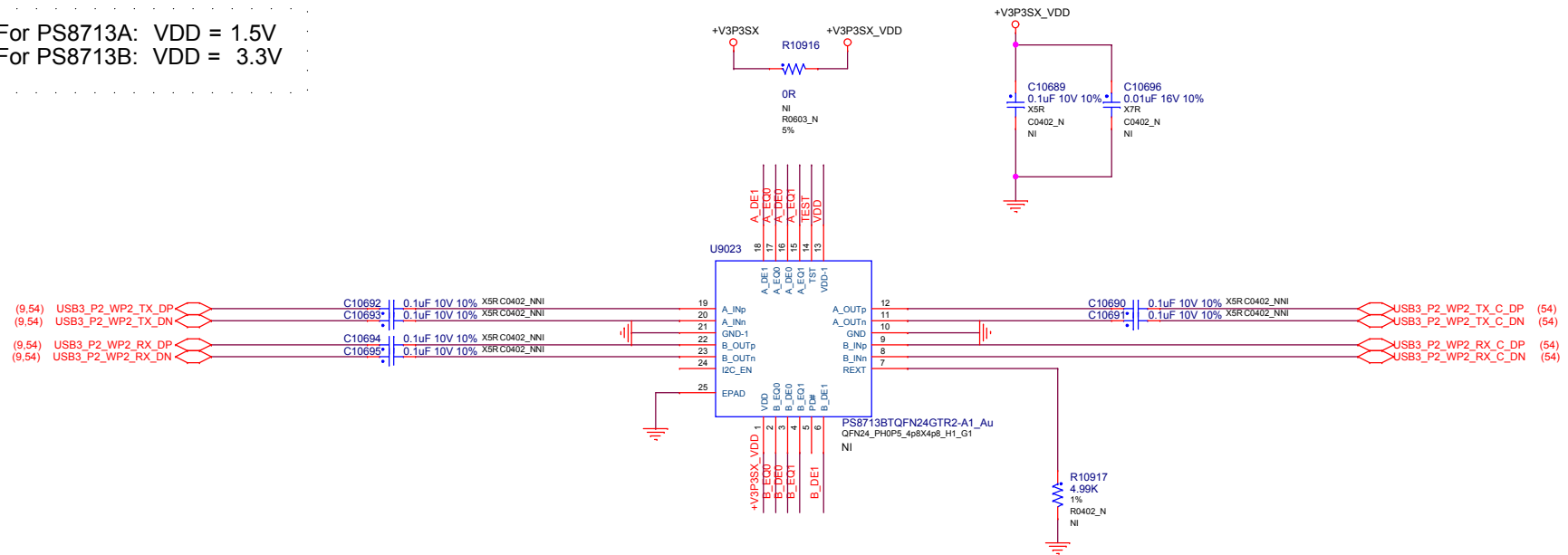


### SYS LED



		Project: 330S-14&15	
		Engineer: Luffy	
Size	Title: BUTTON & LED		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet 51 of 81	

For PS8713A: VDD = 1.5V  
For PS8713B: VDD = 3.3V



A\_EQ0  
A\_EQ1  
R10923 4.7K 5% R0402\_N NI  
R10922 4.7K 5% R0402\_N NI  
+V3P3SX\_VDD

Equalizer control and program for channel A  
3.3V tolerant. Internally pulled down at ~150KΩ  
[A\_EQ1, A\_EQ0] ==  
LL: program EQ for channel loss up to 9.5dB(default)  
LH: program EQ for channel loss up to 13dB  
HL: program EQ for channel loss up to 4.5dB  
HH: program EQ for channel loss up to 7.5dB

A\_DE0  
A\_DE1  
R10918 4.7K 5% R0402\_N NI  
R10919 4.7K 5% R0402\_N NI  
+V3P3SX\_VDD

Programmable output pre-emphasis level setting for channel A  
3.3V tolerant. Internally pulled down at ~150KΩ  
[A\_DE1, A\_DE0] ==  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 2.7dB de-emphasis  
HH: 5dB de-emphasis

B\_EQ0  
B\_EQ1  
R10925 4.7K 5% R0402\_N NI  
R10924 4.7K 5% R0402\_N NI  
+V3P3SX\_VDD


Equalizer control and program for channel B  
3.3V tolerant. Internally pulled down at ~150KΩ  
[B\_EQ1, B\_EQ0] ==  
LL: program EQ for channel loss up to 9.5dB(default)  
LH: program EQ for channel loss up to 13dB  
HL: program EQ for channel loss up to 4.5dB  
HH: program EQ for channel loss up to 7.5dB

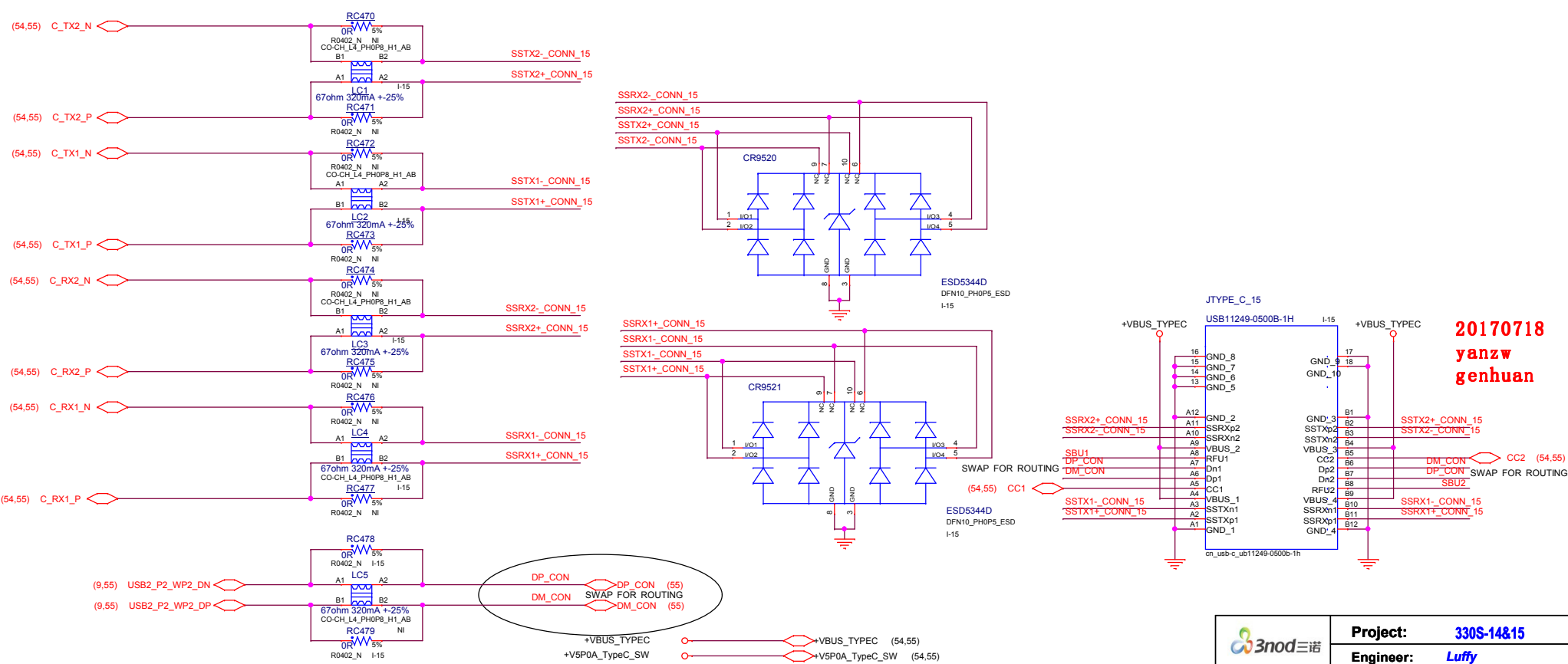
B\_DE0  
B\_DE1  
R10921 4.7K 5% R0402\_N NI  
R10920 4.7K 5% R0402\_N NI  
+V3P3SX\_VDD

Programmable output pre-emphasis level setting for channel B  
3.3V tolerant. Internally pulled down at ~150KΩ  
[B\_DE1, B\_DE0] ==  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 2.7dB de-emphasis  
HH: 5dB de-emphasis

TEST  
R10927 4.7K 5% R0402\_N NI  
+V3P3SX\_VDD

LFPS swing adjust.  
3.3V tolerant. Internally pulled down at ~150KΩ.  
TEST ==  
L: Normal LFPS swing (default)  
H: Turn down LFPS swing

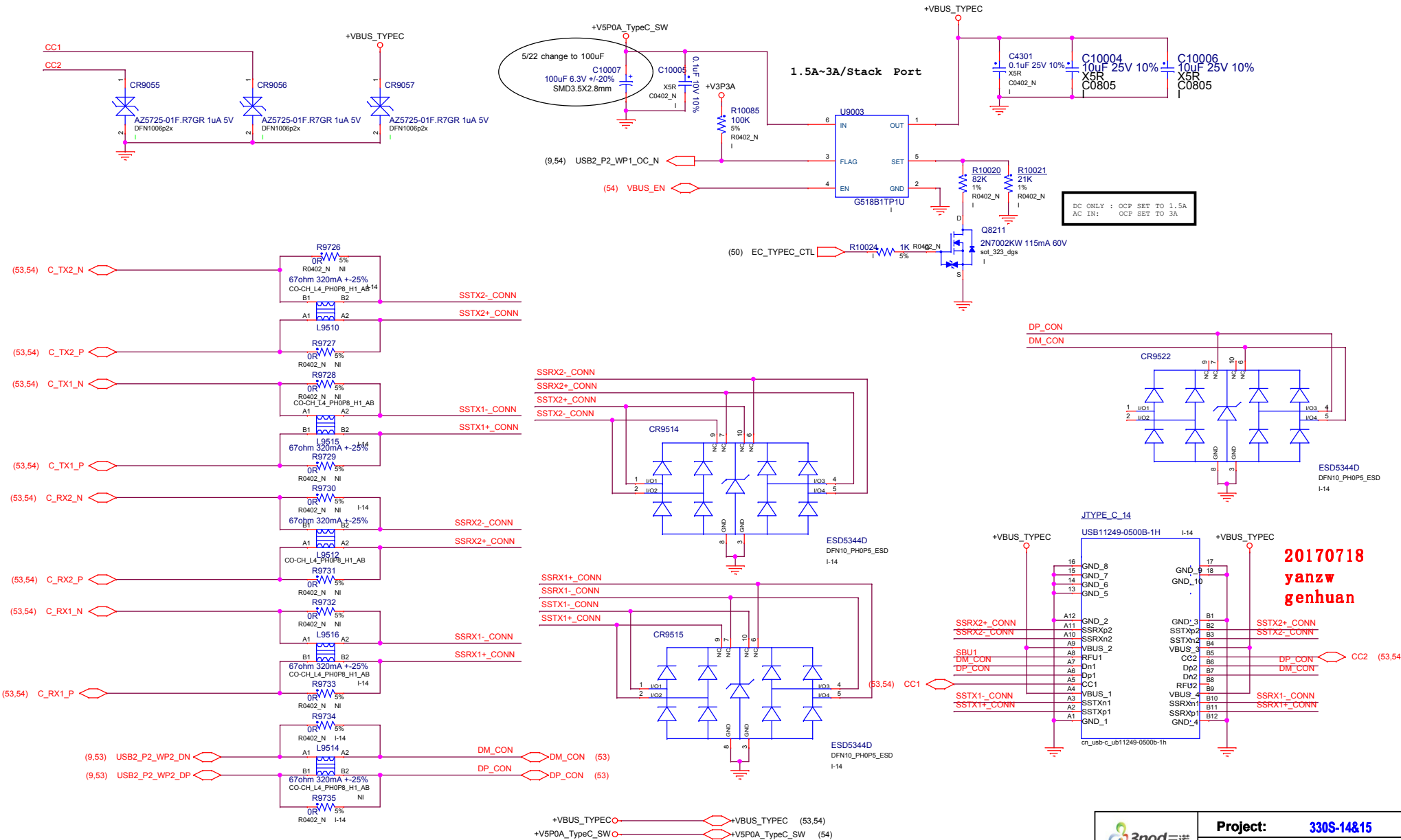
		Project: 330S-14&15
		Engineer: Luffy
Size: Custom	Title: TYPE-C Switch	Rev: V01
Date: Tuesday, September 26, 2017	Sheet: 52 of	81




20170718  
yanzw  
genhuan

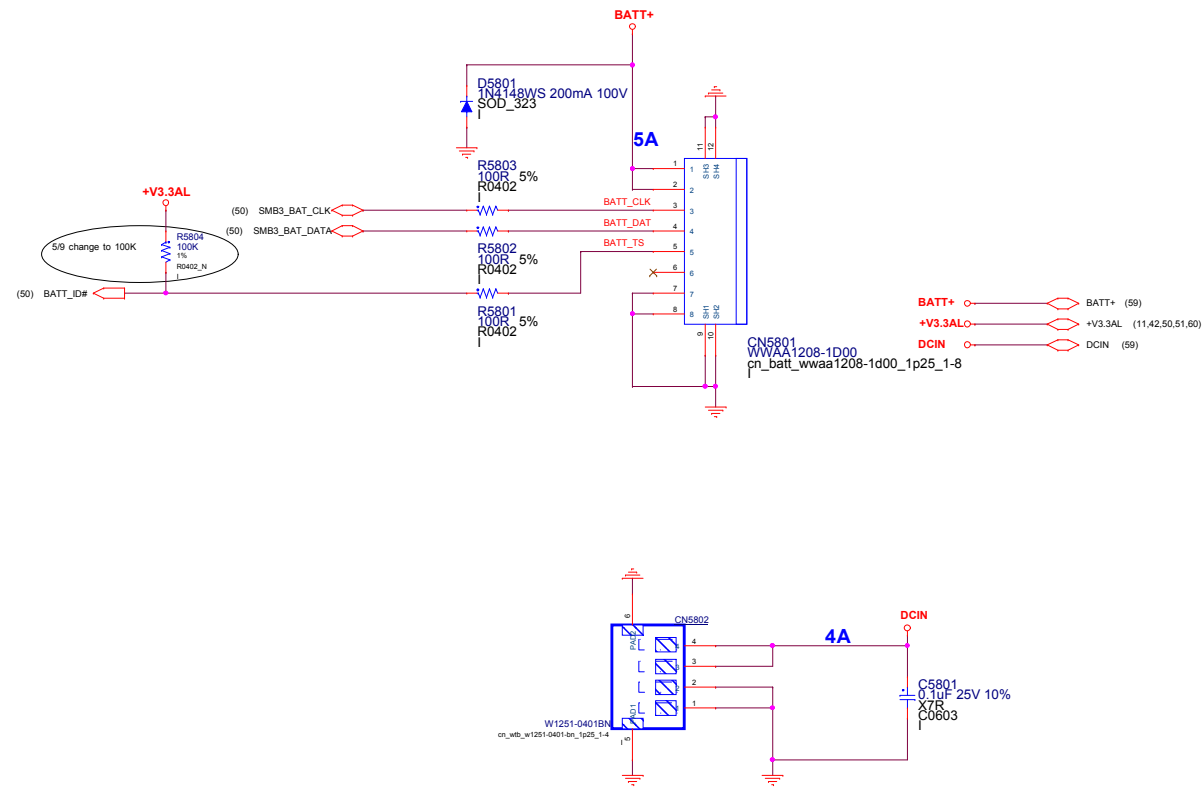
		Project:	330S-14&15
		Engineer:	Luffy
Size	Title: TYPE-C CONN		Rev
Custom			V01
Date:	Tuesday, September 26, 2017		Sheet 53 of 81



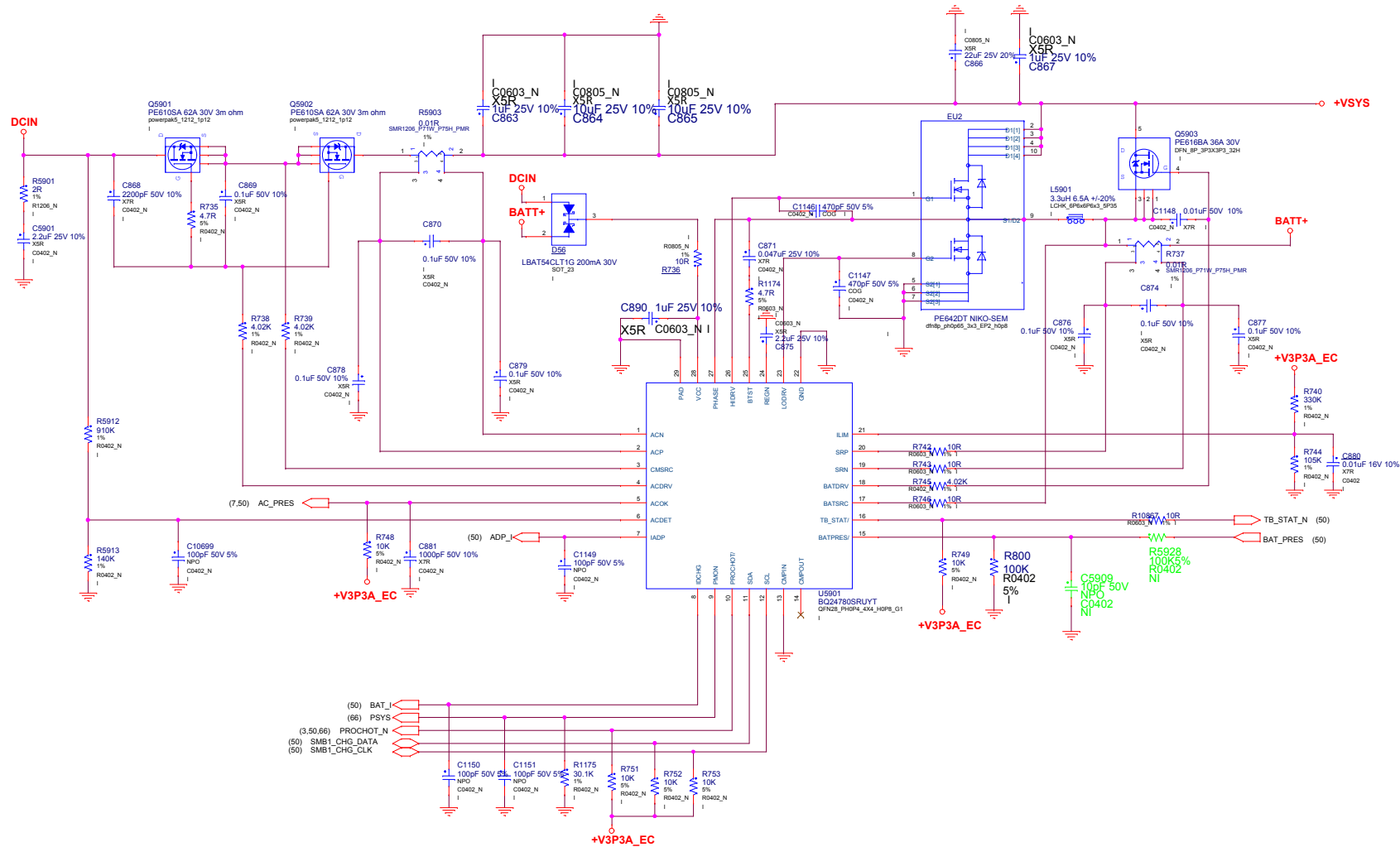


		Project:	330S-14&15
		Engineer:	Luffy
Size	Title: TYPE-C CONN		Rev
Custom			V01
Date:	Tuesday, September 26, 2017		Sheet 55 of 81

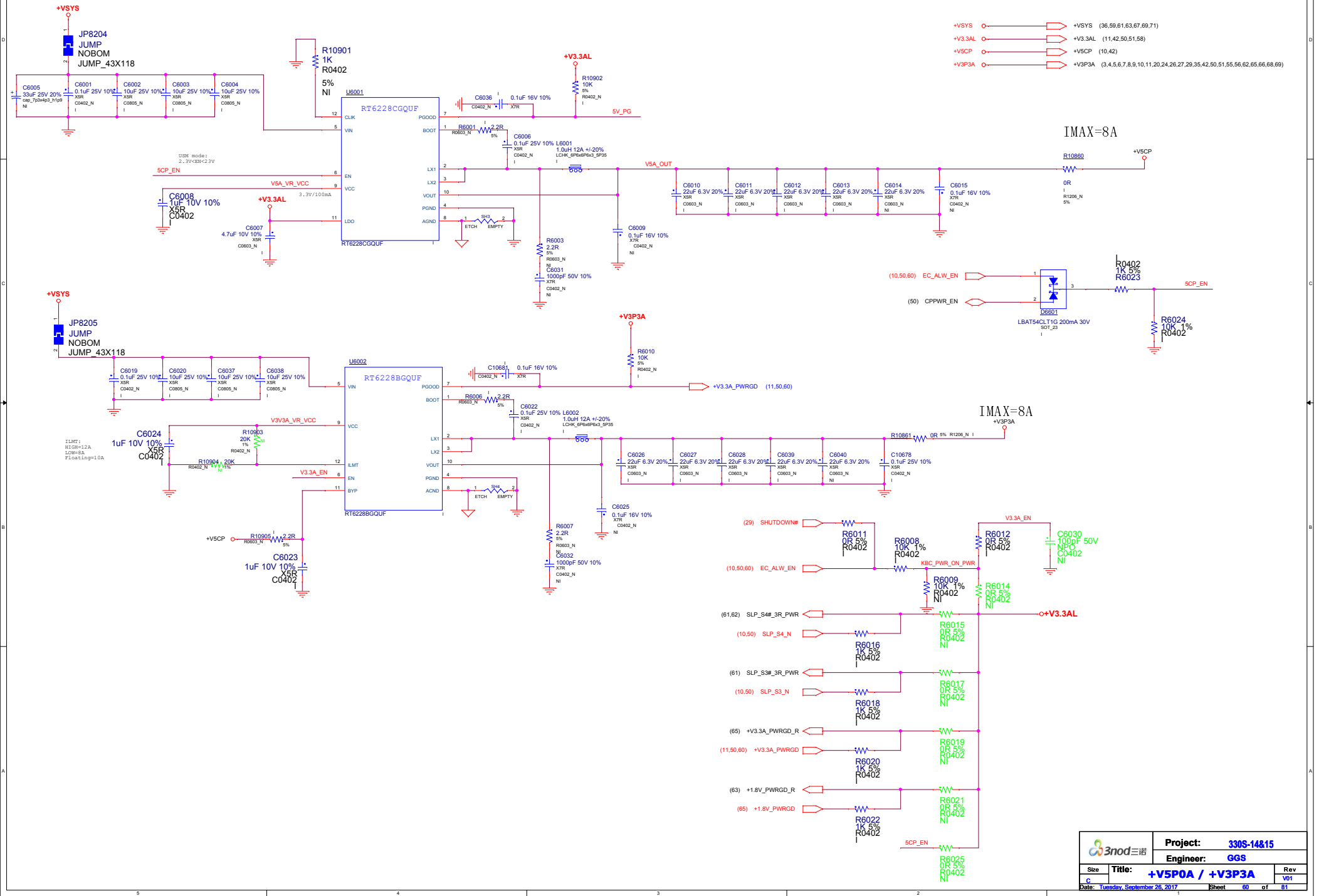
# 58: BATTERY CONNECTOR



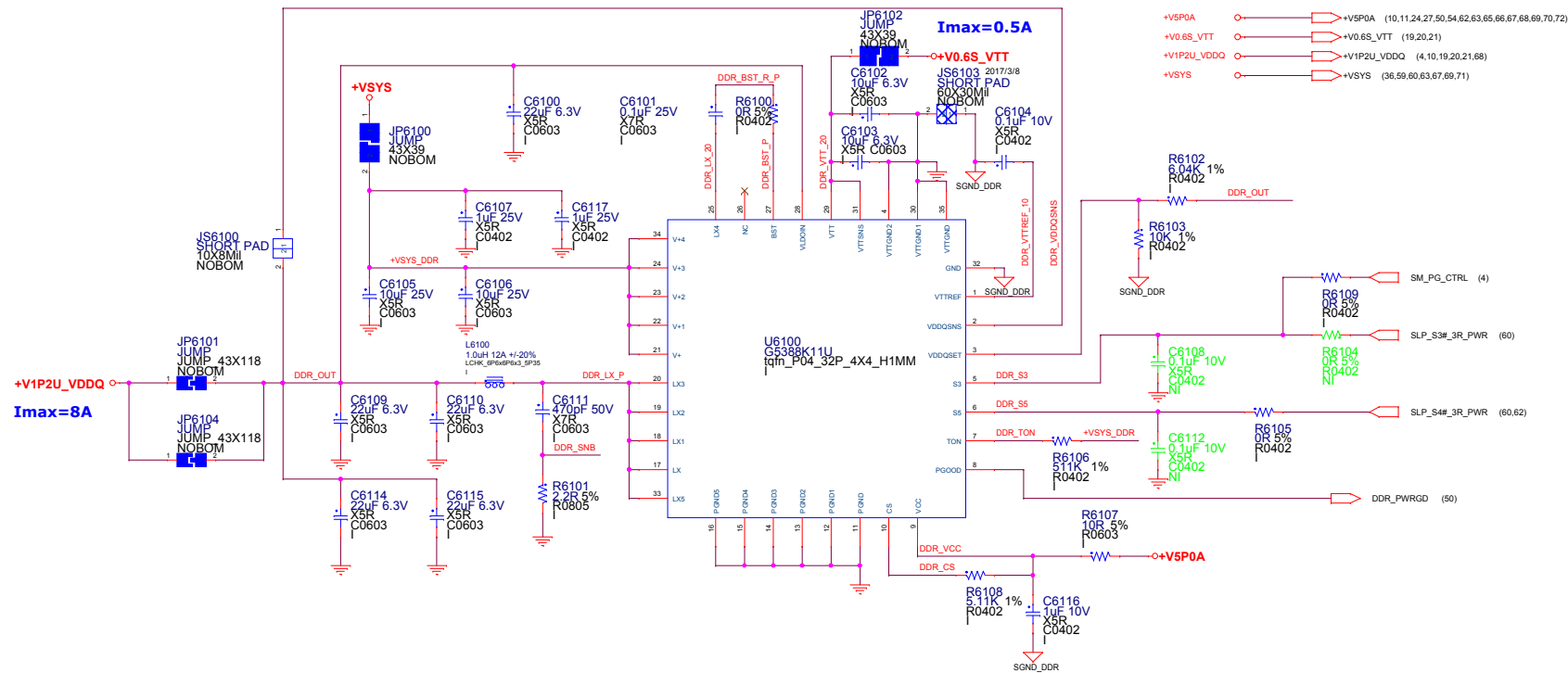
# 59: BATTERY CHARGER



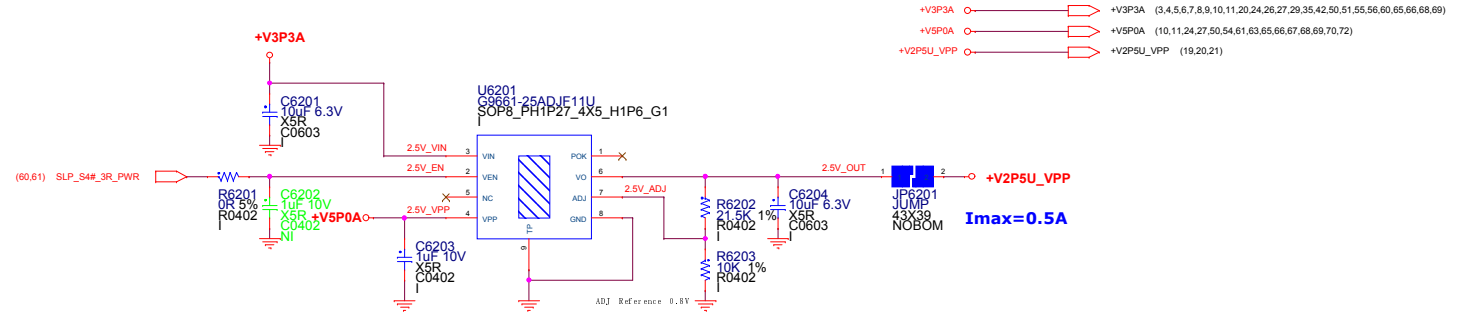
# 60: +V5P0A / +V3P3A POWER SUPPLY



# 61: DDR POWER SUPPLY

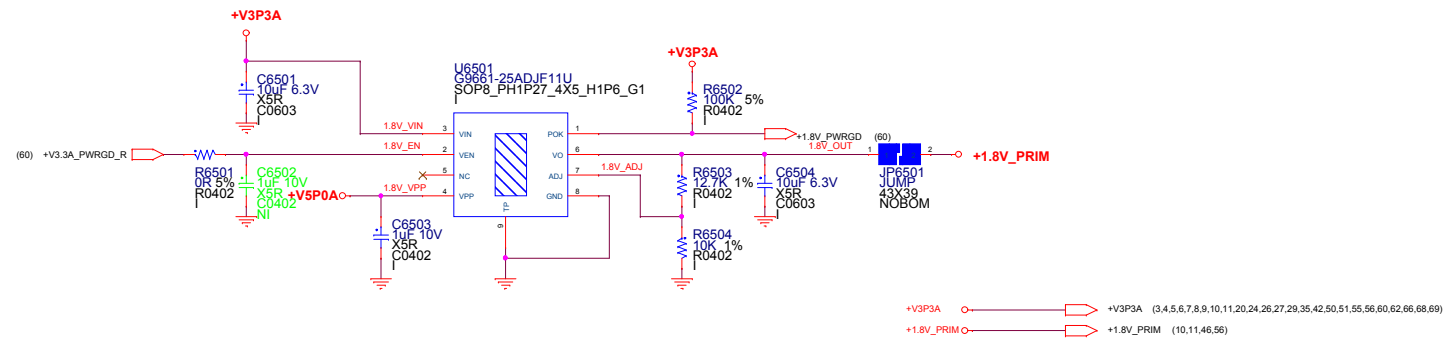


# 62: +V2P5U\_VPP POWER SUPPLY





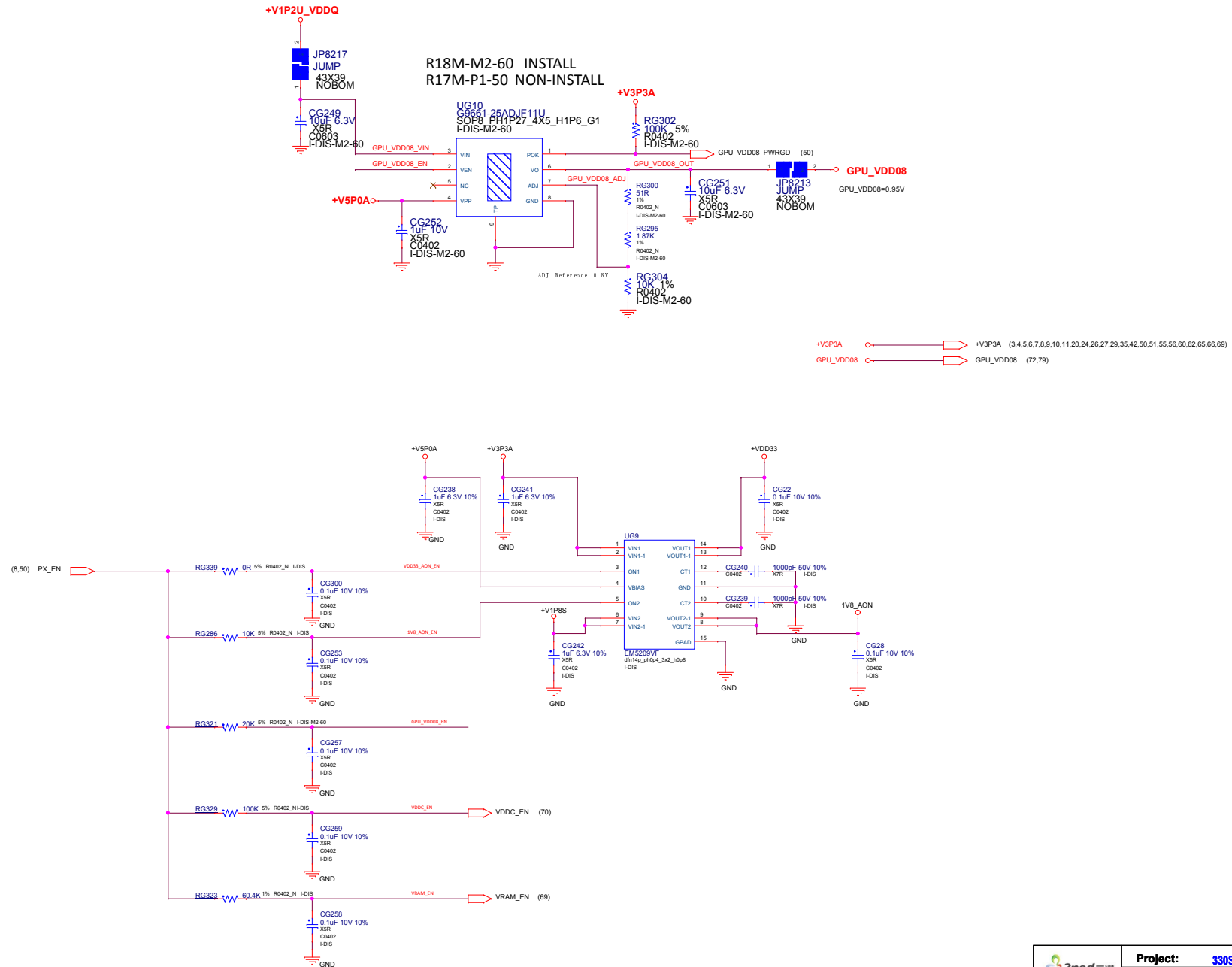
# 65: +1.8V\_PRIM POWER SUPPLY

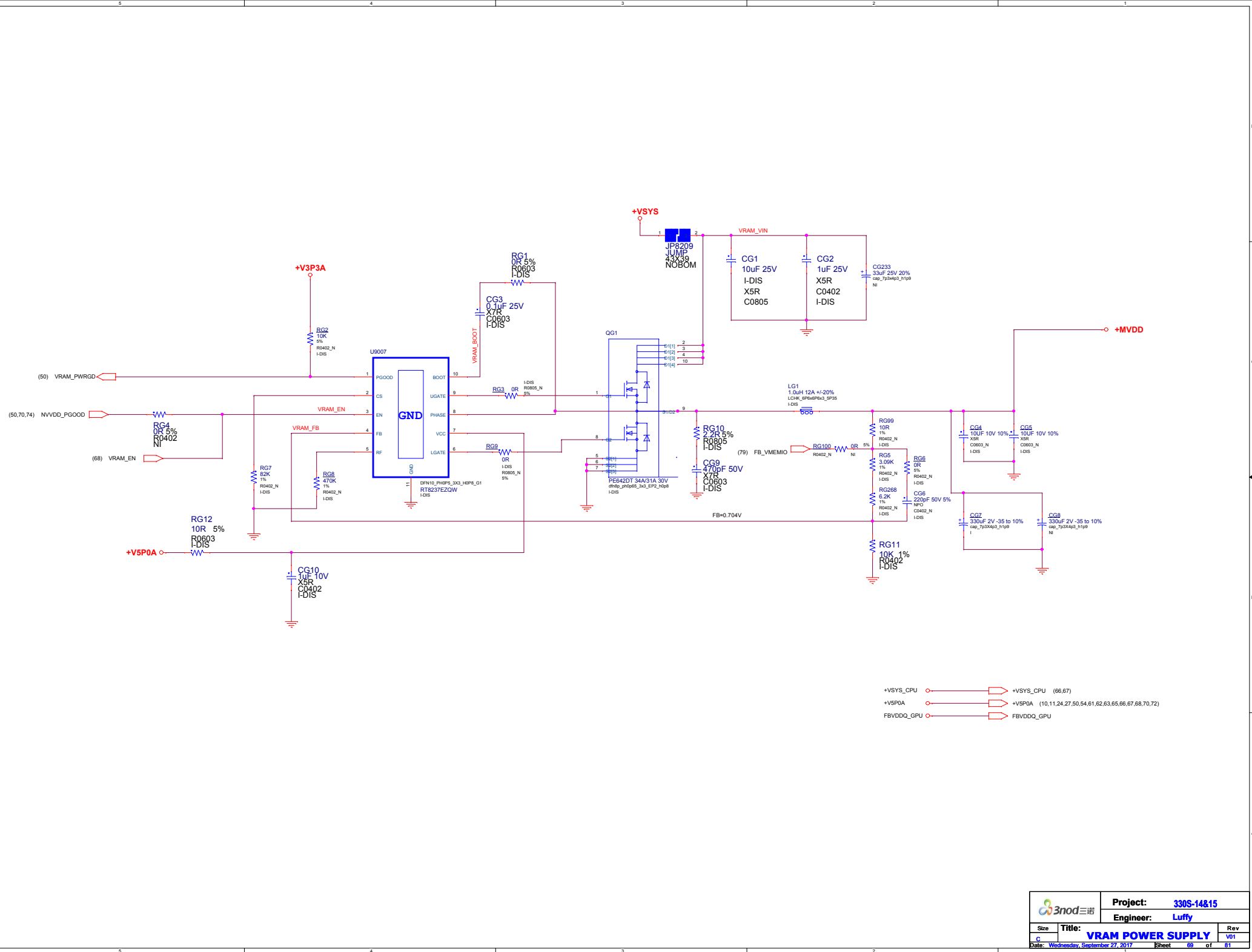






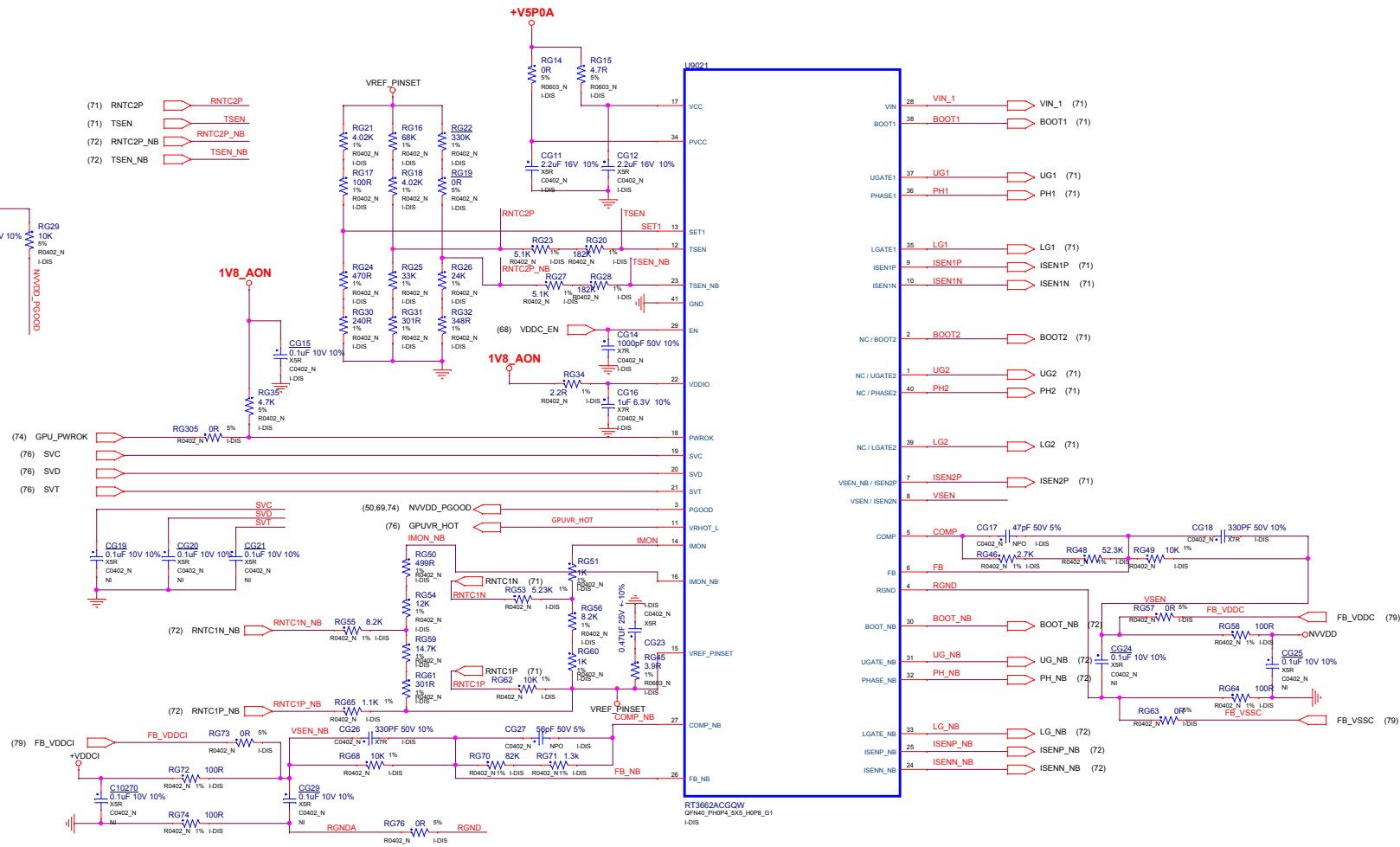
# VDD POWER SUPPLY for M2-60



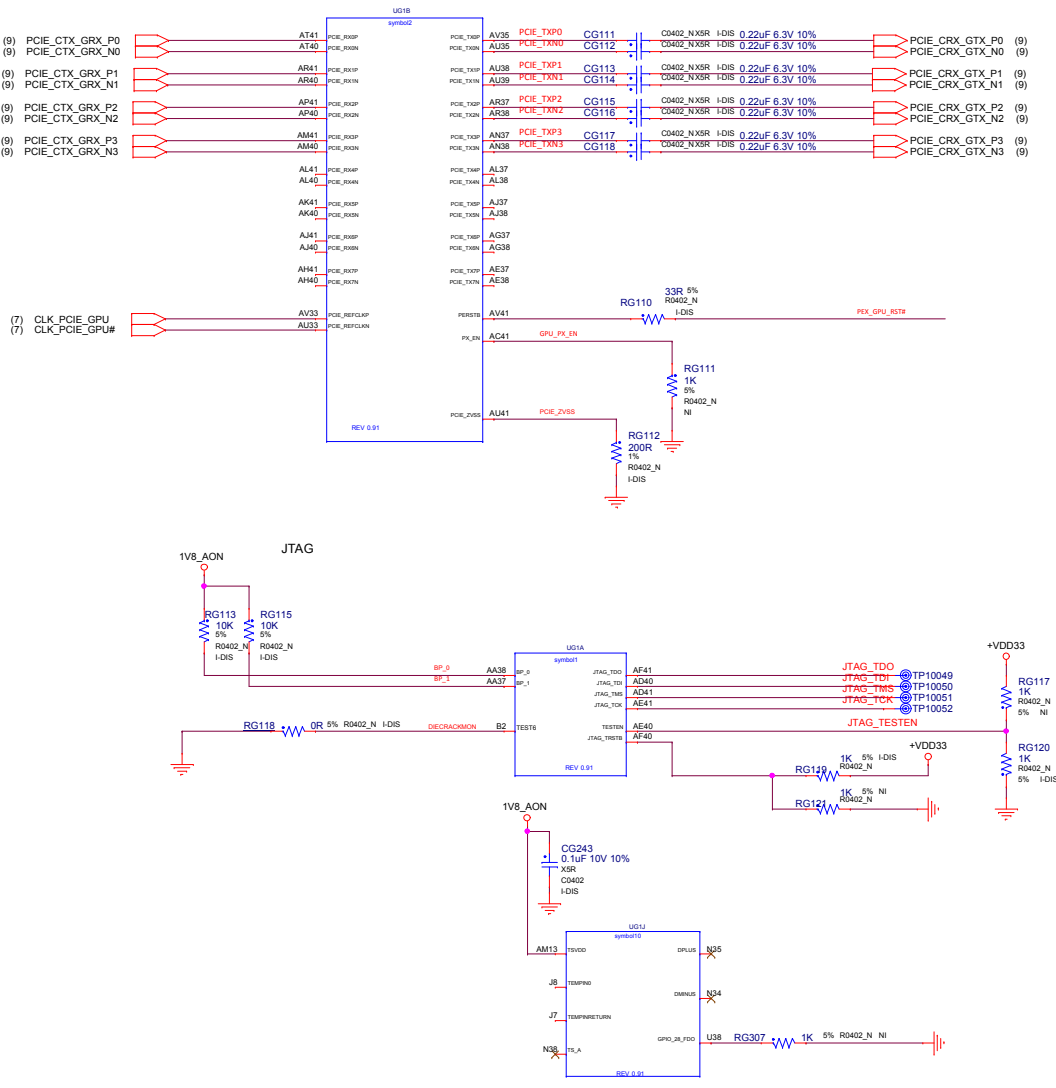
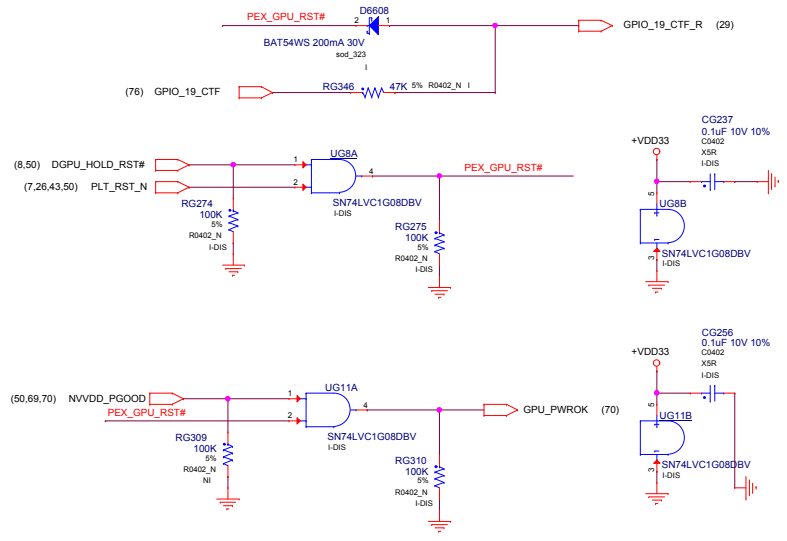


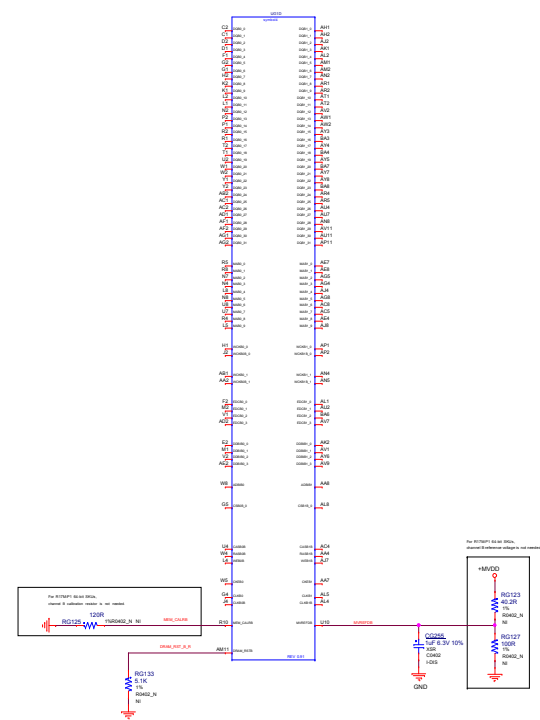
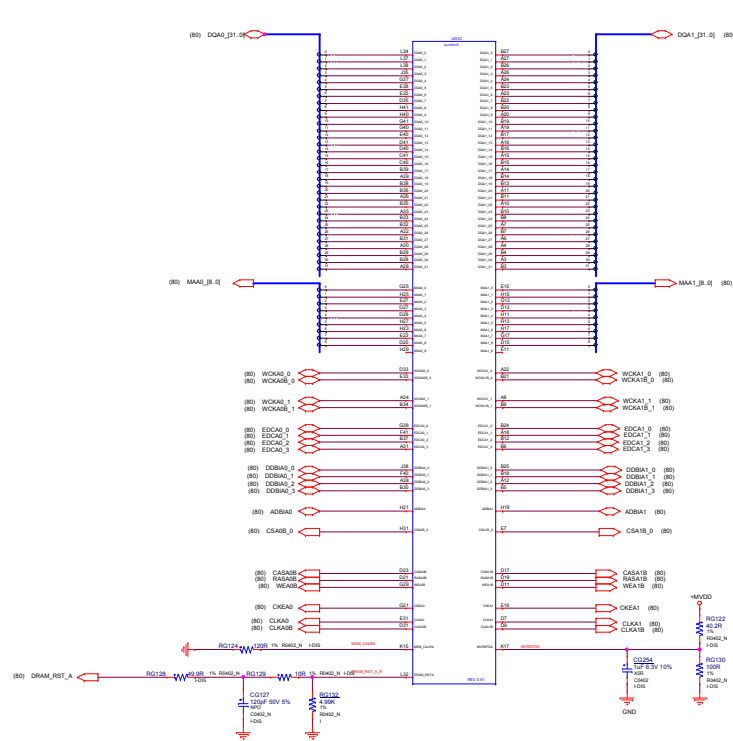
+VSYS\_CPU (66.67) → +VSYS\_CPU (66.67)  
+V5P0A (10.11,24.27,50.54,61.62,63.65,66.67,68,70,72) → +V5P0A (10.11,24.27,50.54,61.62,63.65,66.67,68,70,72)  
FBVDDQ\_GPU → FBVDDQ\_GPU

# 70: GPU POWER



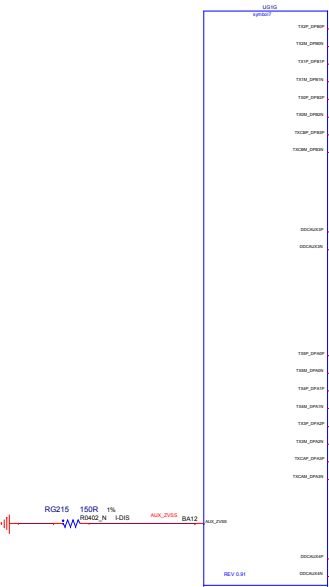








ASIC - TMDP (A/B)



ASIC - TMDP (C/D)

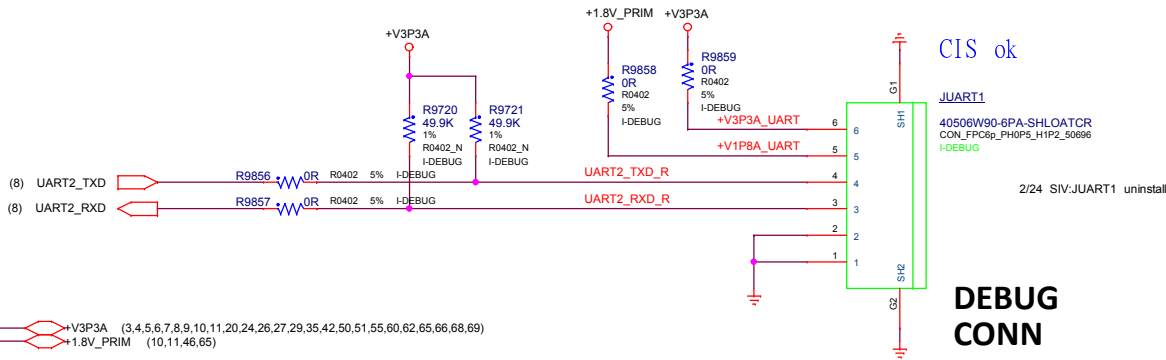


ASIC - TMDP (E)



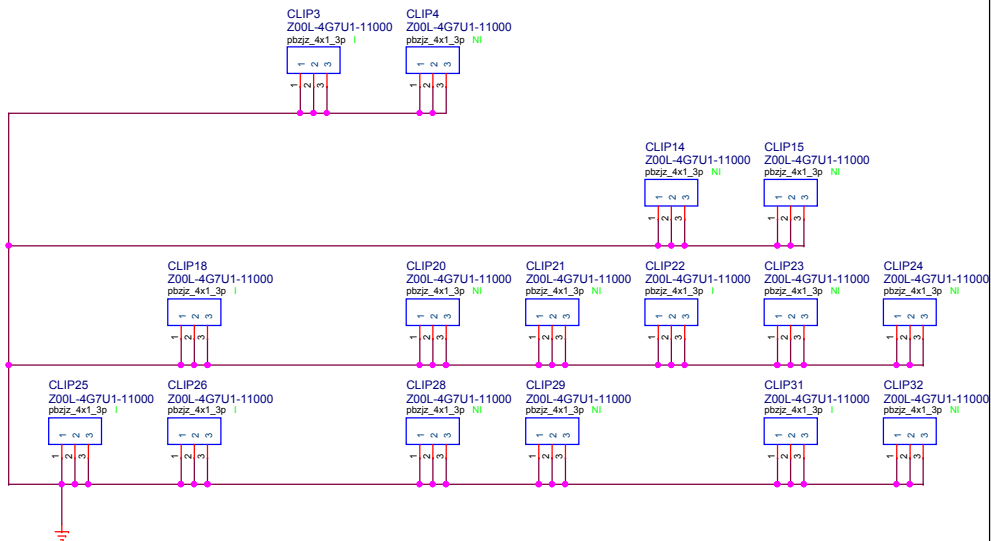




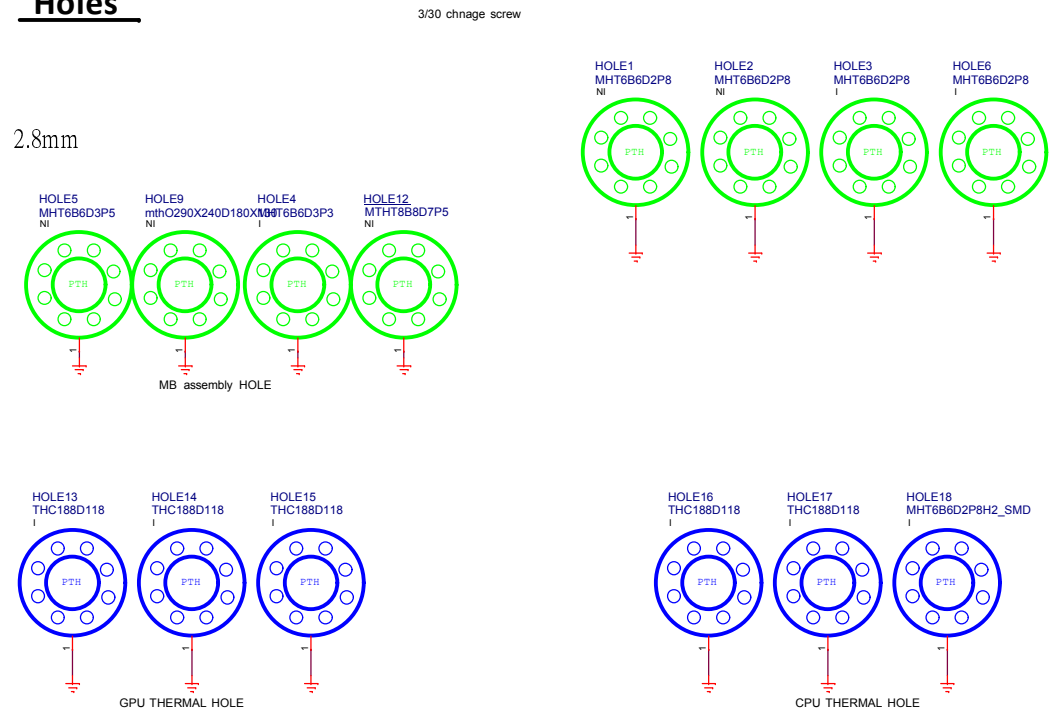


+V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,60,62,65,66,68,69)  
+1.8V\_PRIM (10,11,46,65)

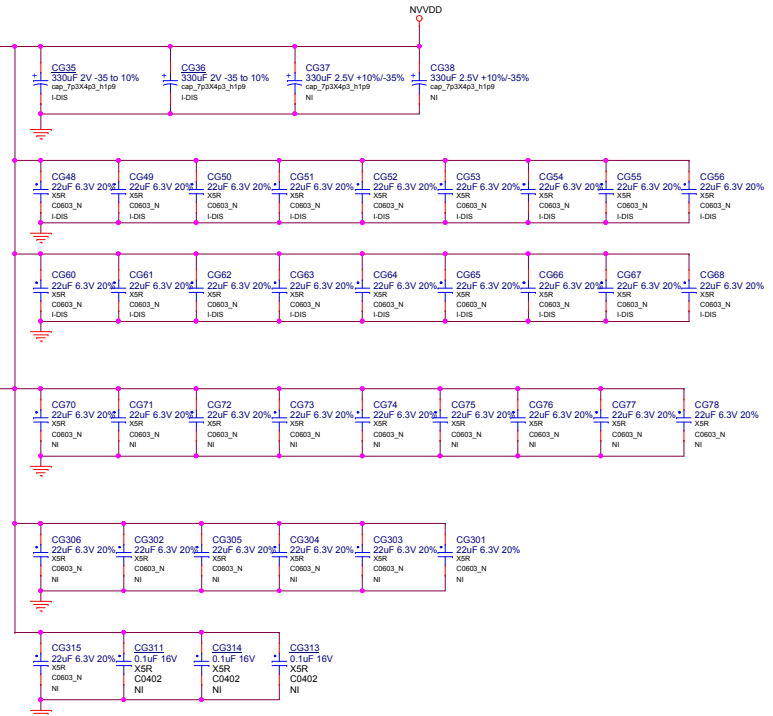
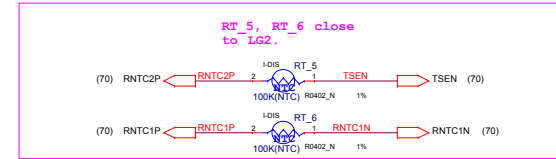
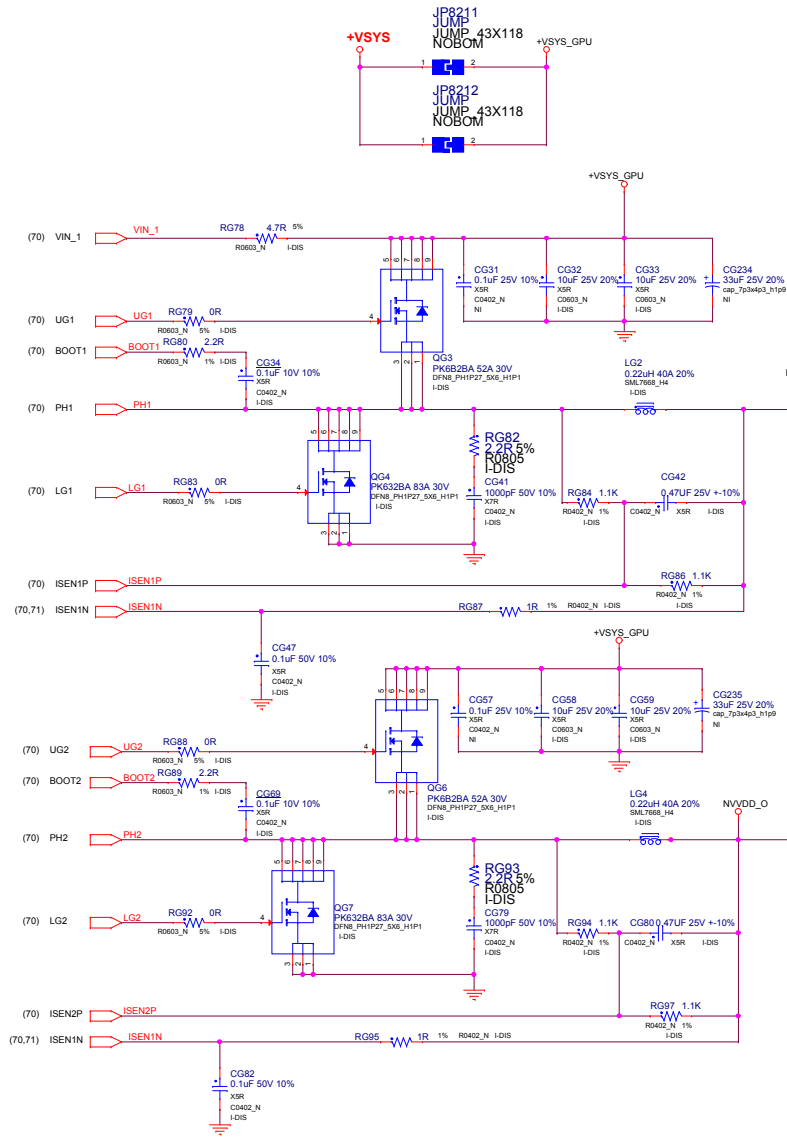
## Shielding

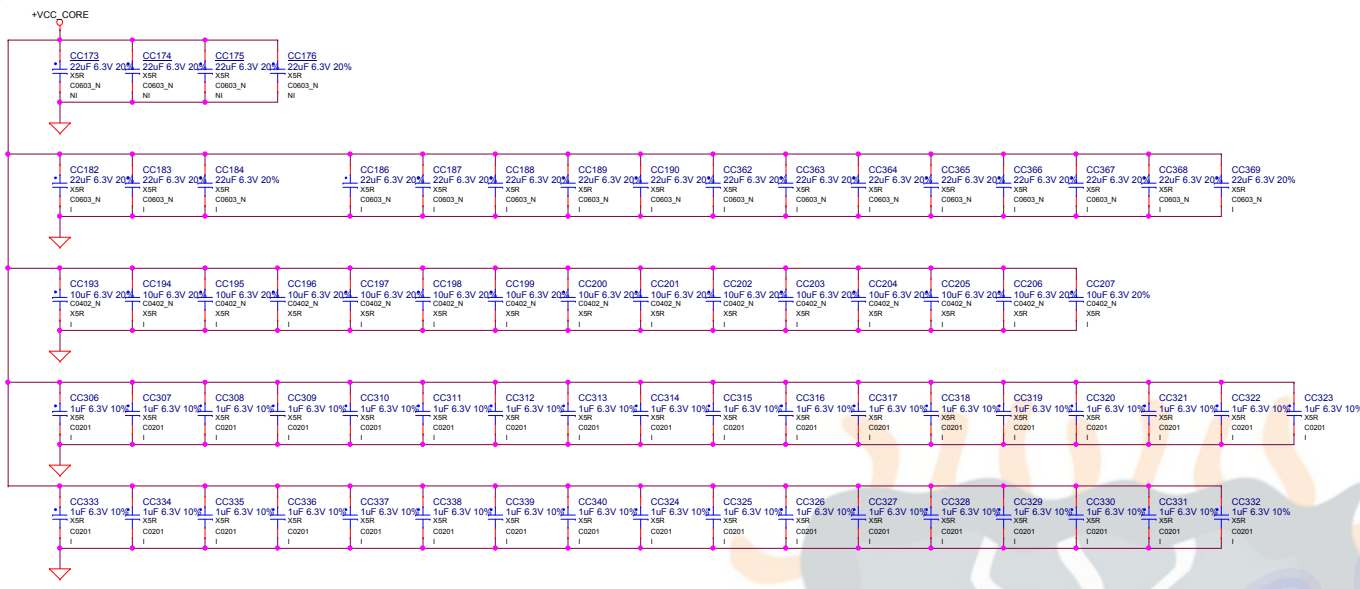


## Holes



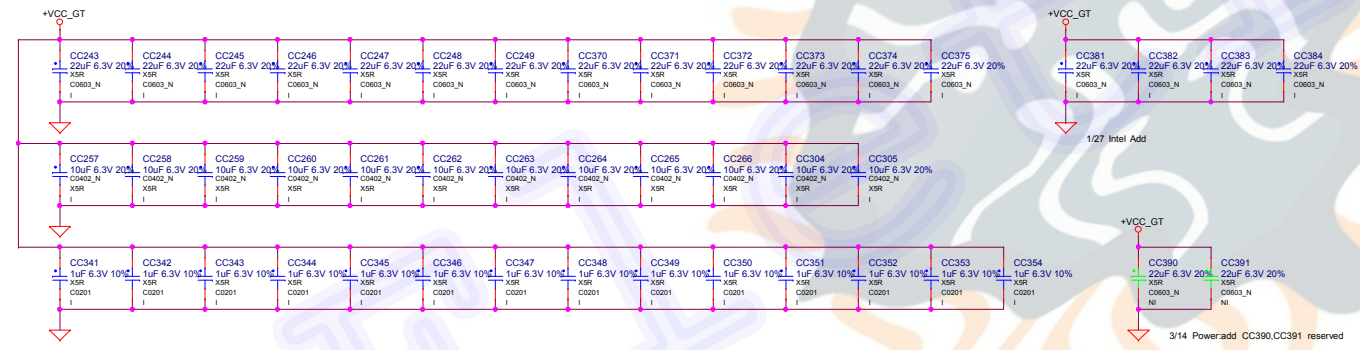
		<b>Project:</b> 330S-14&15	
		<b>Engineer:</b> Luffy	
Size	<b>Title:</b> UART CONN & HOLE & CLIP		Rev
Custom			V01
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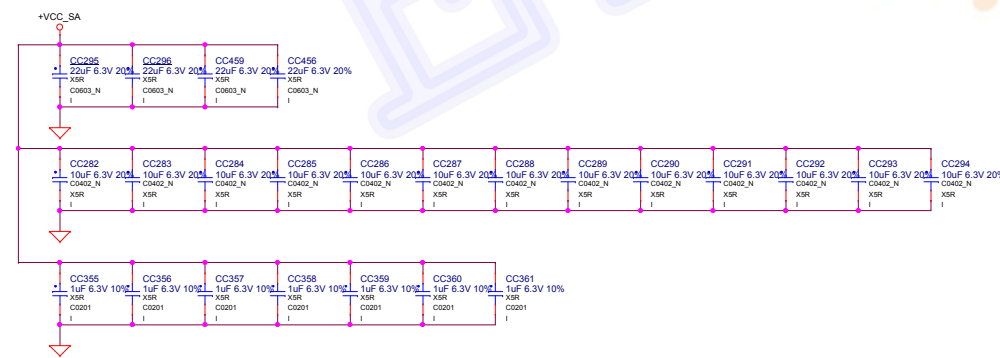
12/30 check PDG  
& 220uF pull power side

**+VCC\_CORE**  
 47uF x8 change 47uF x4  
 22uF x9 cgange 22uF x17  
 10uF x15  
 1uF x35



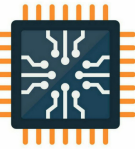
12/30 check PDG  
& 220uF pull power side

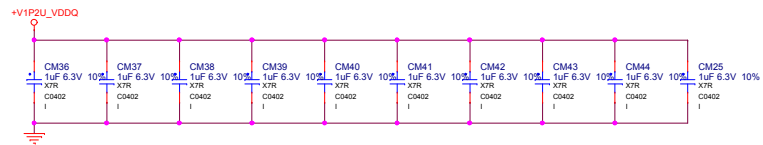
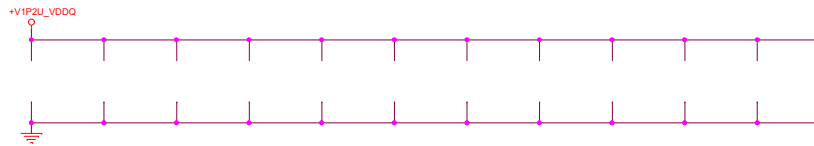
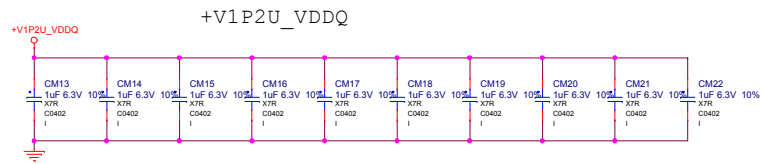
**+VCC\_GT**  
 47uF x3 change 47uF x0  
 22uF x7 cgange 22uF x13  
 10uF x12  
 1uF x14



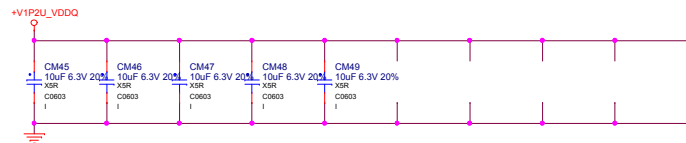
12/30 check PDG

**+VCC\_SA**  
 47uF x2  
 10uF x13  
 1uF x7



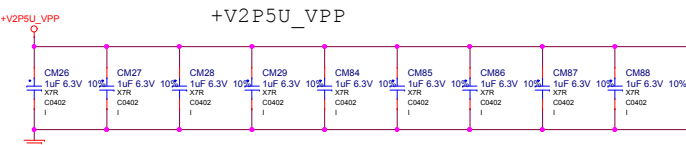
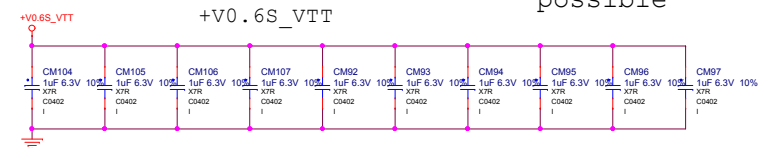


1uF:4 as near each x16  
DRAM device as  
possible

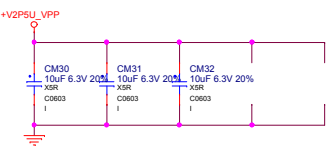
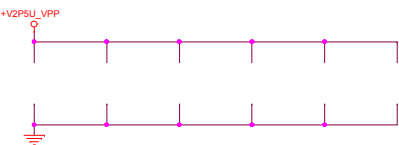


10uF:Distributed around  
the DRAM devices

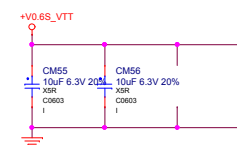
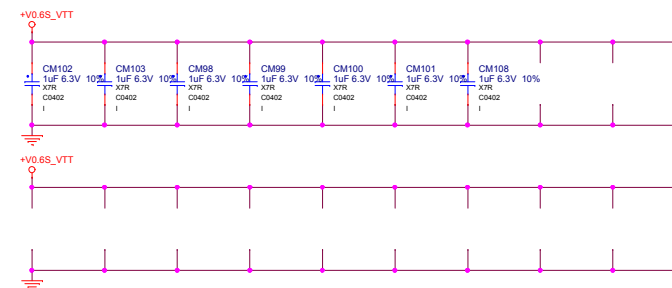
1uF:2 as near each x20  
DRAM device as  
possible



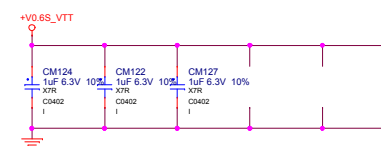
1uF:2 as near each x16  
DRAM device as  
possible



10uF:Distributed around  
the DRAM devices



10uF:Distributed around  
the DRAM devices



3/31 add CAPs

+V1P2U\_VDDQ (4.10,19.20,61.68)  
+V2P5U\_VPP (19.20,62)  
+V0.6S\_VTT (19.20,61)

Project: 330S-14&15		Rev	
Engineer: Luffy		V01	
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